



05N50-SE2

Preliminary

Power MOSFET

**0.5A, 500V N-CHANNEL
POWER MOSFET**

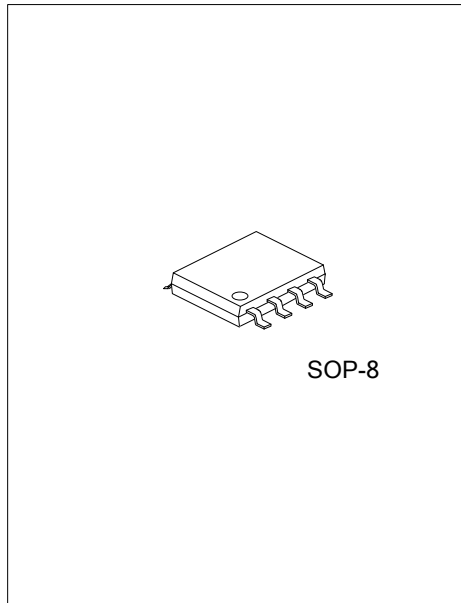
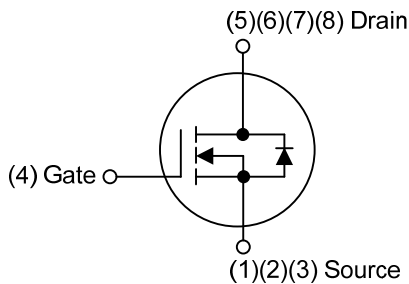
■ DESCRIPTION

The UTC **05N50-SE2** is a high voltage MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.

■ FEATURES

- * $R_{DS(ON)} \leq 15 \Omega$ @ $V_{GS}=10V, I_D=0.25A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

■ SYMBOL



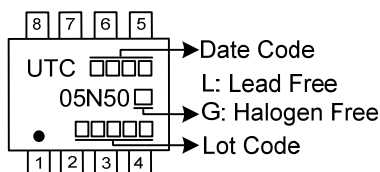
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
05N50L-S08-R	05N50G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>05N50G-S08-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8</p> <p>(3) G: Halogen Free and Lead Free L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	0.5	A
	Pulsed (Note 2)	I_{DM}	1	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.2	V/ns
Power Dissipation		P_D	1.6	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $I_{SD} \leq 0.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	90	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	78.1	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

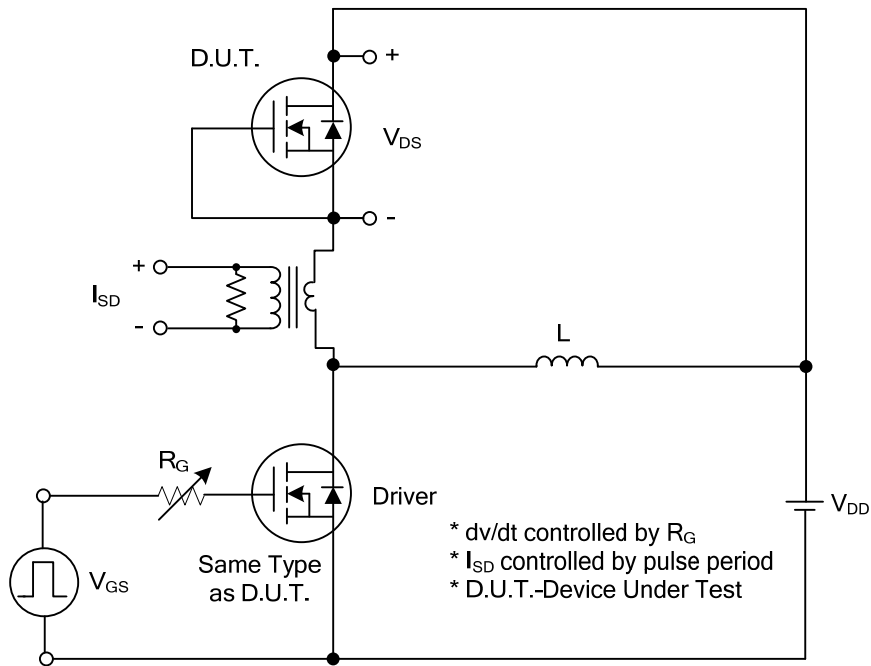
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	I_{GSS}	Forward			100	nA
		Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$		-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=0.25\text{A}$			15	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$		57		pF
Output Capacitance	C_{OSS}			13		pF
Reverse Transfer Capacitance	C_{RSS}			2		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		7		nC
Gate to Source Charge	Q_{GS}			2		nC
Gate to Drain Charge	Q_{GD}			0.5		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		6		ns
Rise Time	t_R			16		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			25		ns
Fall-Time	t_F			36		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Maximum Body-Diode Continuous Current	I_S				0.5	A
Maximum Body-Diode Pulsed Current (Note 1)	I_{SM}				1	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=0.5\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$I_S=0.5\text{A}$, $V_{GS}=0\text{V}$		140		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$		406		nC

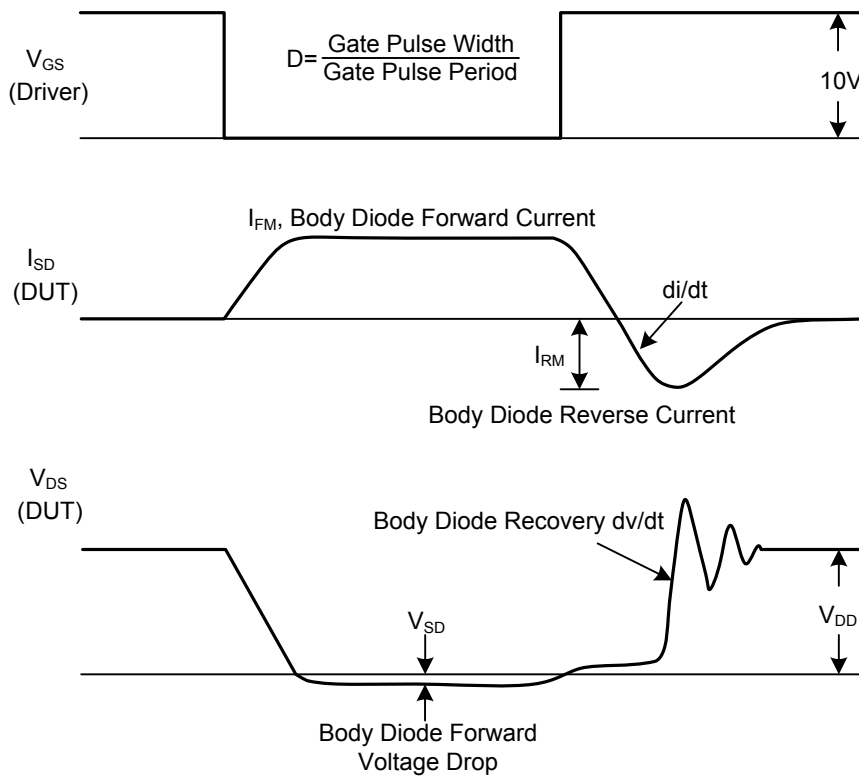
Notes: 1. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

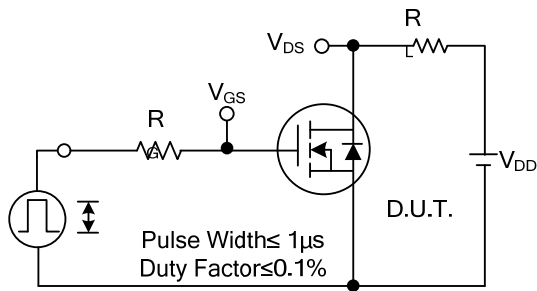


Peak Diode Recovery dv/dt Test Circuit

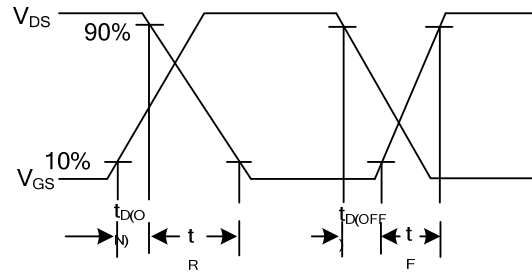


Peak Diode Recovery dv/dt Waveforms

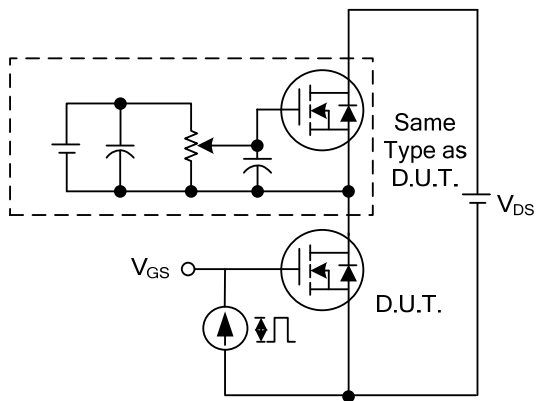
■ TEST CIRCUITS AND WAVEFORMS



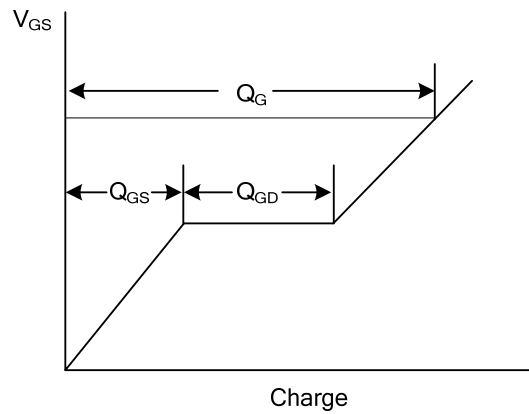
Switching Test Circuit



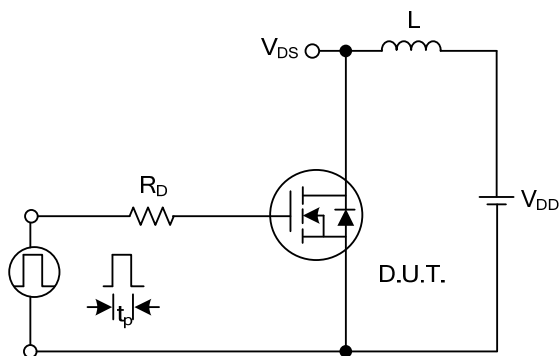
Switching Waveforms



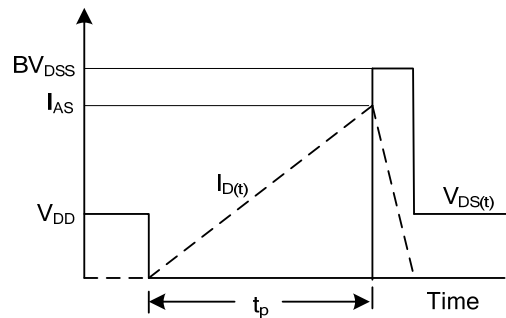
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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