



UT10P15

Preliminary

POWER MOSFET

-10A, -150V P-CHANNEL POWER MOSFET

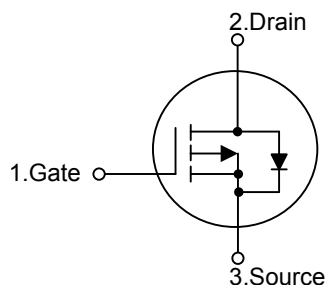
DESCRIPTION

The **UT10P15** uses advanced proprietary, planar stripe, DMOS technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable to be used in low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

FEATURES

- * $R_{DS(ON)} \leq 0.35 \Omega$ @ $V_{GS} = -10V$, $I_D = -5.0A$
 $R_{DS(ON)} \leq 0.40 \Omega$ @ $V_{GS} = -4.5V$, $I_D = -5.0A$
- * High Switching Speed
- * High Cell Density Trench Technology

SYMBOL



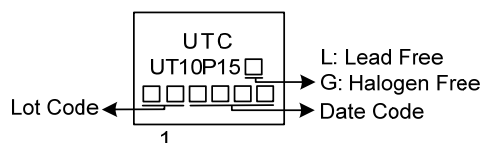
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT10P15L-TN3-R	UT10P15G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT10P15G-TN3-R 		(1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	-150	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-10	A
Pulsed Drain Current (Note 2)	I_{DM}	-20	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	32	mJ
Peak Diode Recovery dv/dt	dv/dt	5.2	V/ns
Power Dissipation	P_D	42	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=-25\text{A}$, $V_{DD}=-50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

4. $I_{SD}\leq -10\text{A}$, $di/dt \leq 200\mu\text{A/s}$, $V_{DD}\leq BV_{DS}$, Starting $T_J=25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C/W}$
Junction to Case	θ_{JC}	2.97 (Note)	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

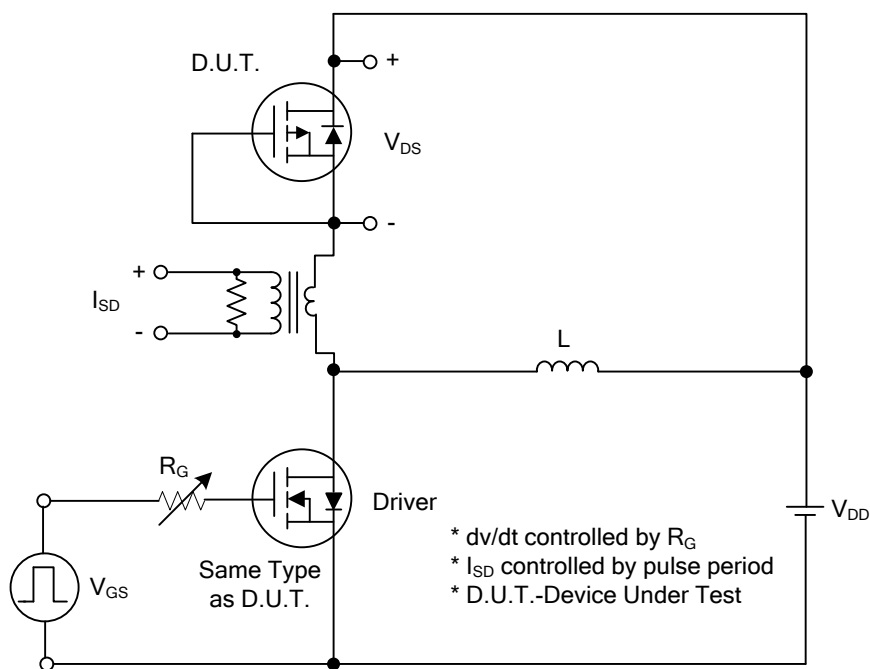
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0 V, I _D =-250μA	-150			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-150V, V _{GS} =0V			-10	μA
		V _{DS} =-150V, T _C =125°C			-10	μA
Gate-Source Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-5.0A			0.35	Ω
		V _{GS} =-4.5V, I _D =-5.0A			0.40	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =-25V, V _{GS} =0V, f=1.0MHz		1150		pF
Output Capacitance	C _{OSS}			90		pF
Reverse Transfer Capacitance	C _{RSS}			46		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =-120V, V _{GS} =-10V, I _D =-10A I _G =-1mA (Note 1, 2)		28		nC
Gate Source Charge	Q _{GS}			6		nC
Gate Drain Charge	Q _{GD}			8		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =-75V, V _{GS} =-10V, I _D =-10A, R _G =6Ω (Note 1, 2)		7		ns
Turn-ON Rise Time	t _R			17.5		ns
Turn-OFF Delay Time	t _{D(OFF)}			40		ns
Turn-OFF Fall-Time	t _F			26		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				-10	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				-20	A
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-10A			-1.4	V
Body Diode Reverse Recovery Time	t _{rr}	V _{GS} = 0V, I _S =-10A,		90		ns
Body Diode Reverse Recovery Charge	Q _{rr}	di _F /dt=100A/μs (Note 1)		0.3		μC

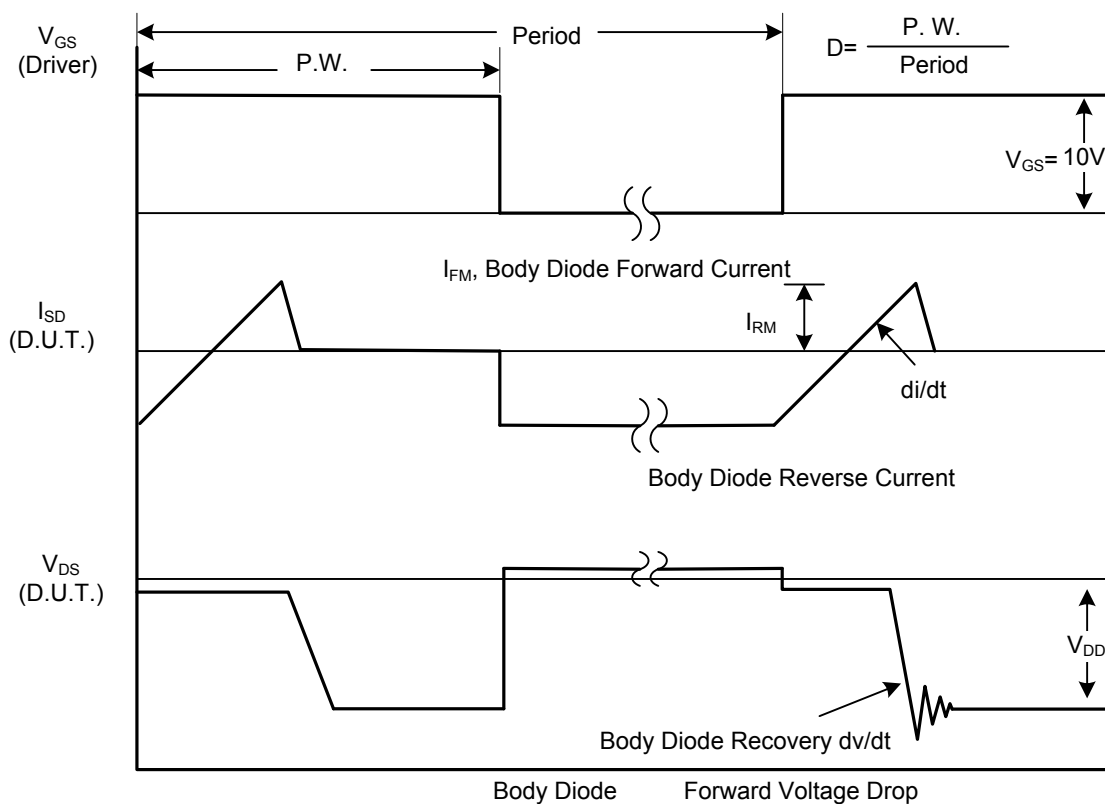
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

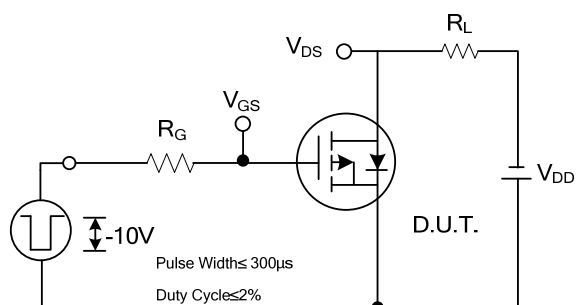


Peak Diode Recovery dv/dt Test Circuit

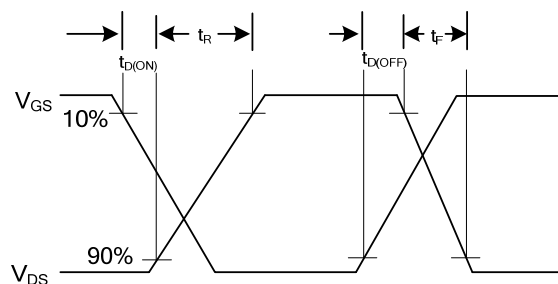


Peak Diode Recovery dv/dt Waveforms

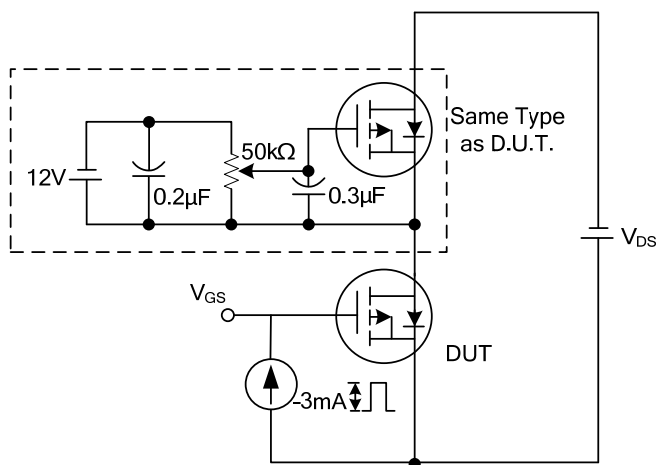
■ TEST CIRCUITS AND WAVEFORMS



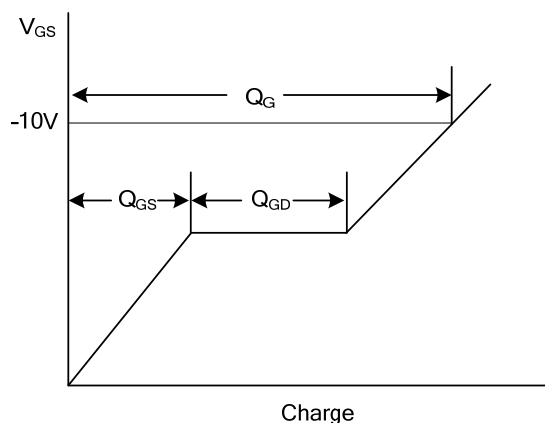
Switching Test Circuit



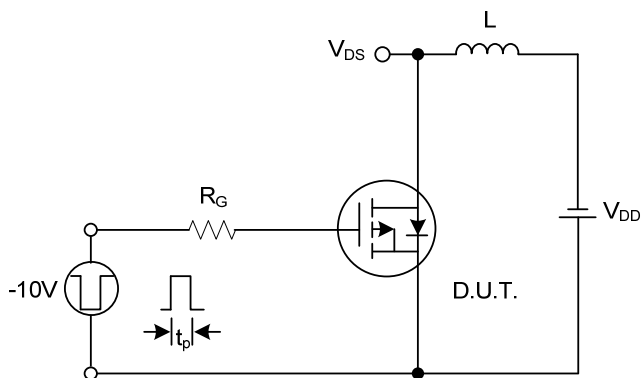
Switching Waveforms



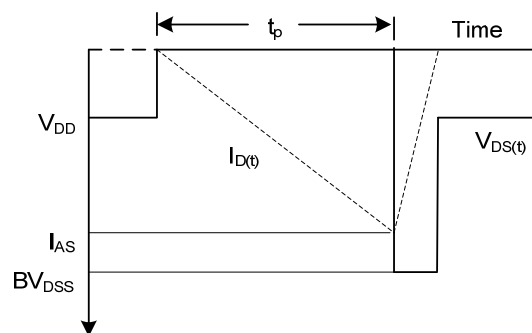
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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