



## UT9PP03

Preliminary

Power MOSFET

### P-CHANNEL ENHANCEMENT MODE POWER MOSFET

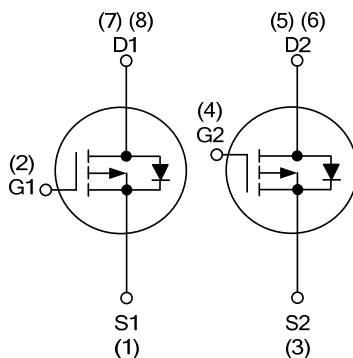
#### DESCRIPTION

The **UT9PP03** uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

#### FEATURES

- \*  $R_{DS(ON)} \leq 18 \text{ m}\Omega$  @  $V_{GS} = -10\text{V}$ ,  $I_D = -4.5\text{A}$
- \*  $R_{DS(ON)} \leq 26 \text{ m}\Omega$  @  $V_{GS} = -4.5\text{V}$ ,  $I_D = -4.5\text{A}$
- \* Low capacitance
- \* Low gate charge
- \* Fast switching capability
- \* Avalanche energy specified

#### SYMBOL



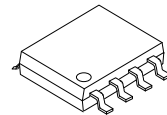
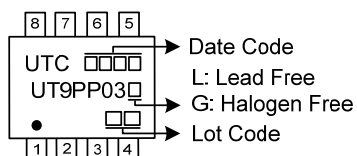
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT9PP03L-S08-R	UT9PP03G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<b>UT9PP03G-S08-R</b>		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) S08: SOP-8
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

#### MARKING



SOP-8

■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	-9	A
Pulsed Drain Current (Note 2)	$I_{DM}$	-18	A
Avalanche Energy	$E_{AS}$	79	mJ
Single Pulsed (Note 3)			
Power Dissipation	$P_D$	1.8	W
Junction Temperature	$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3.  $L = 0.1\text{mH}$ ,  $I_{AS} = -39.8\text{A}$ ,  $V_{DD} = -30\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}\text{C}$ .

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	90	$^{\circ}\text{C/W}$
Junction to Case	$\theta_{JC}$	69	$^{\circ}\text{C/W}$

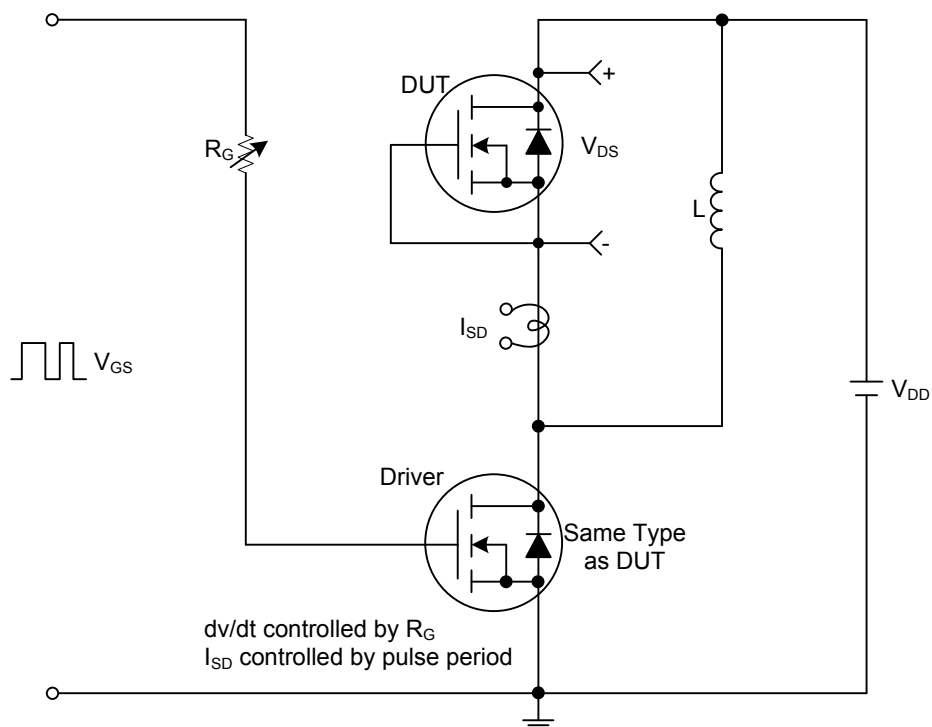
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise specified)

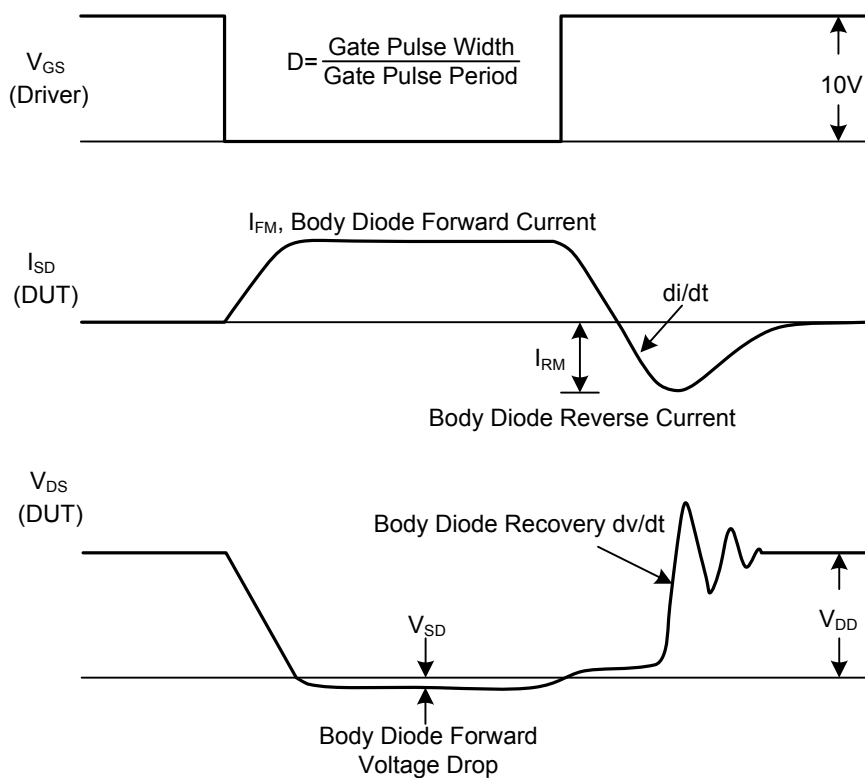
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V			-1	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =-250μA	-1.0		-3.0	V
Static Drain-Source On-Resistance (Note)	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.5A			18	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =4.5A			26	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-25V, V <sub>GS</sub> =0V, f=1.0MHz		2280		pF
Output Capacitance	C <sub>OSS</sub>			365		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			328		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note)	Q <sub>G</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A		29		nC
Gate Source Charge	Q <sub>GS</sub>			5		nC
Gate Drain Charge	Q <sub>GD</sub>			13.5		nC
Turn-ON Delay Time (Note)	t <sub>D(ON)</sub>	V <sub>DS</sub> =-30V, I <sub>D</sub> =-20A, V <sub>GS</sub> =-10V R <sub>G</sub> =3.3Ω, R <sub>D</sub> =15Ω		9.5		ns
Turn-ON Rise Time	t <sub>R</sub>			21		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			84		ns
Turn-OFF Fall-Time	t <sub>F</sub>			55		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V			-1.2	V

Note: Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .

# ■ TEST CIRCUITS AND WAVEFORMS



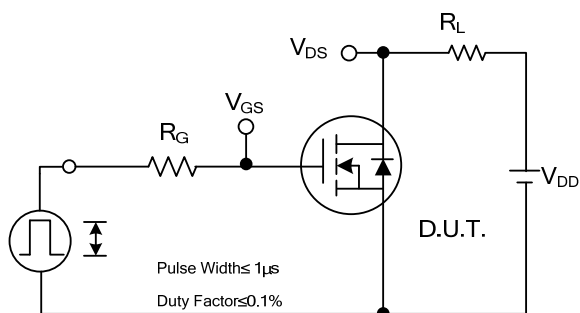
**Peak Diode Recovery dv/dt Test Circuit**



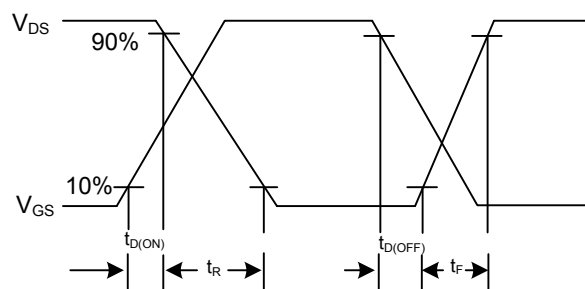
**Peak Diode Recovery dv/dt Test Circuit and Waveforms**

**Peak Diode Recovery dv/dt Waveforms**

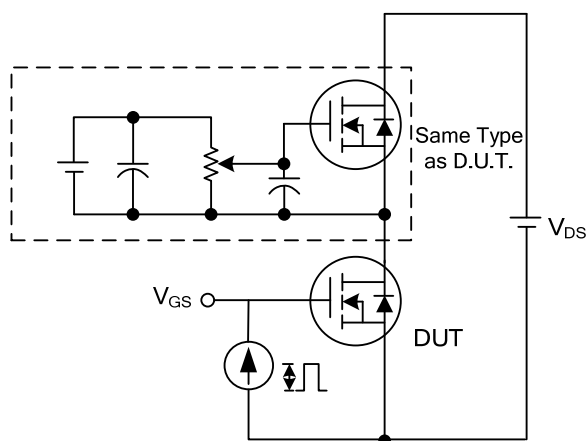
# ■ TEST CIRCUITS AND WAVEFORMS



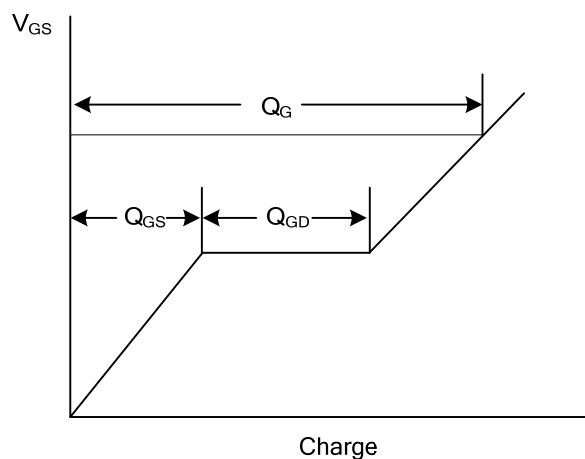
Switching Test Circuit



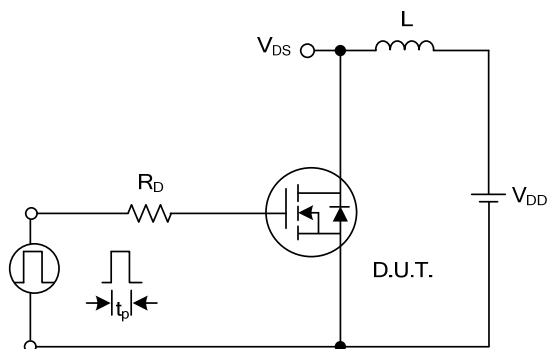
Switching Waveforms



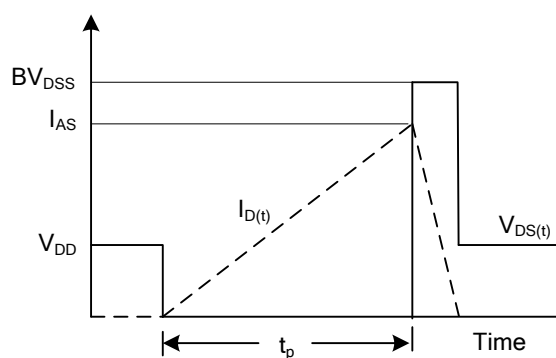
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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