4 STAGE FET LNA BIAS CONTROLLER

QFN-16(3x3)

■ DESCRIPTION

The UTC **L8403** is an advanced GaAs and HEMT FETs bias controller. It is designed to operate from minimal supply rails and intended primarily for satellite Low Noise Blocks (LNBs).

The UTC **L8403** provides drain voltage and current control for up to 4 external grounded source FETs with the addition of one capacitor and two resistors.

The UTC **L8403** is generating the regulated negative rail required for FET gate biasing whilst operating from a single supply of 2.1V to 5.5V.

The -2V negative bias can also be used to supply other external circuits. The UTC **L8403** uses two resistors to split control between two pairs of FETs and set drain currents. This allows the operating current of input FETs to be adjusted to minimize noise, whilst the following FET stages can separately be adjusted for maximum gain.

■ FEATURES

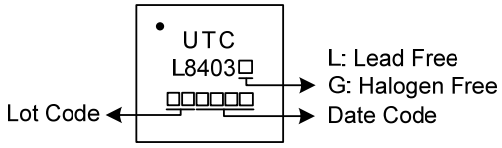
* Provides Bias for up to 4 GaAs and HEMT FETs
* Operating Range of 2.1V to 5.5V
* Ultra-low Operating Current of 0.95mA
* Dynamic FET Protection
* Amplifier FET Drain Voltages set at 2.0V
* Regulated Negative Rail Generator Requires only 1 External Capacitor
* Expended Temperature Range of -40°C to +105°C

■ ORDERING INFORMATION

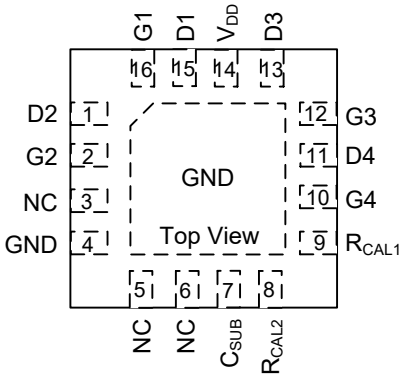
Ordering Number		Package	Packing
Lead Free	Halogen Free		
L8403L-Q16-3030-R	L8403G-Q16-3030-R	QFN-16(3×3)	Tape Reel

L8403G-Q16-3030-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) Q16-3030: QFN-16(3×3) (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



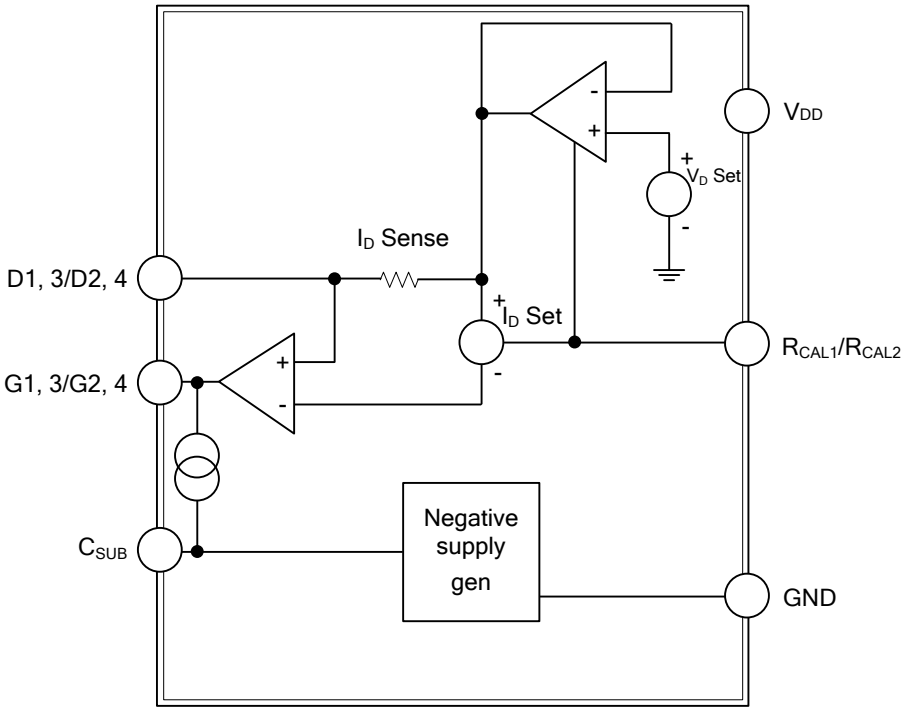
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	D2	To Drain of FET 2
2	G2	To Gate of FET 2
3	NC	No Connection
4	GND	Ground
5	NC	No Connection
6	NC	No Connection
7	C_{SUB}	Negative rail reservoir capacitor
8	R_{CAL2}	Drain current setting for D2 and D4
9	R_{CAL1}	Drain current setting for D1 and D3
10	G4	To Gate of FET 4
11	D4	To Drain of FET 4
12	G3	To Gate of FET 3
13	D3	To Drain of FET 3
14	V_{DD}	Supply voltage
15	D1	To Drain of FET 1
16	G1	To Gate of FET 1
Pad	GND	Must be connected to Ground or No Connection

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.6 ~ +6	V
Supply Current	I_{DD}	100	mA
Power Dissipation	P_D	650	mW
Junction Temperature	T_J	+135	°C
Storage Temperature Range	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Note 5)

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage Range	V_{DD}	2.1 ~ 5.5	V
Operating Temperature Range	T_A	-40 ~ +105	°C

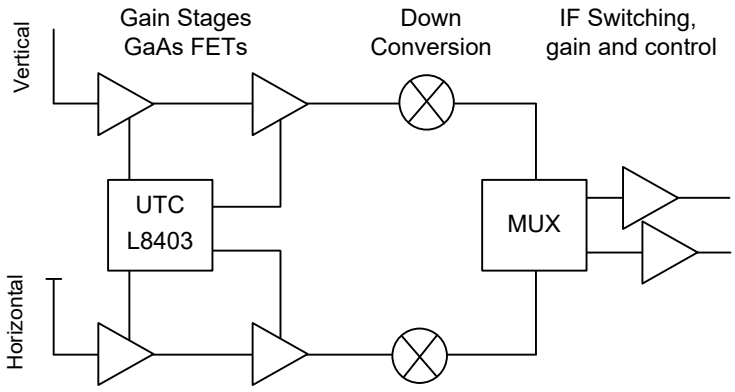
■ ELECTRICAL CHARACTERISTICS

(T_A=25°C, V_{DD}=2.3V, R_{CAL1}=R_{CAL2}=33kΩ, setting I_{D1} to I_{D4} set to 10mA.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current	I_{DD}	I_{D1-4}=0		0.95	2.0	mA
	$I_{DD(L)}$	I_{D1-4}=10mA			45	mA
Substrate Voltage (Note 2)	V_{CSUB}	I_{CSUB}=0	-2.5	-2.0	-1.5	V
	$V_{CSUB(L)}$	I_{CSUB}=-20μA			-1.5	V
GATE CHARACTERISTICS						
Gate (G1 to G4)						
Current Range	I_G		-50		60	μA
Voltage Low	$V_{G(L)}$	I_D=12mA, I_G=-10μA	-2.5	-2.0	-1.5	V
Voltage High	$V_{G(H)}$	I_D=8.0mA, I_G= 0	0	0.7	1.0	V
DRAIN CHARACTERISTICS						
Drain (D1 to D4)						
Current Range	I_D	D1 and D4	4		15	mA
Current Operating (Note 1)	$I_{D(OP)}$	Standard Application Circuit	8	10	12	mA
Voltage Operating (Note 4)	$V_{D(OP)}$	I_D=9.0mA	1.8	2.0	2.2	V
delta V_D vs. V_{DD}	dV_D/dV_{DD}	V_{DD} = 2.3V~5.5V		0.15		%/V
delta I_D vs. V_{DD}	dI_D/dV_{DD}	V_{DD} = 2.3V~ 5.5V		1.5		%/V
delta V_D vs. T_A	dV_D/dT_A	T_A = -40°C~+105°C		150		ppm

Notes: 1. Characteristics are measured using up to two external reference resistors, R_{CAL1} and R_{CAL2}.
2. The negative bias voltages are generated on-chip using an internal oscillator. An external 47nF capacitor is required for this purpose.
3. Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.
4. The maximum operating drain voltage is equal to V_{DD} or $V_{D(OP)}$ max whichever is lower.
5. ESD sensitive, handling precautions are recommended.

■ TWIN LNB SYSTEM DIAGRAM



■ DEVICE DESCRIPTION

The UTC **L8403** is designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs with a minimum of external components whilst operating from a minimal voltage supply and using minimal current.

The UTC **L8403** has four FET bias stages that can be programmed to provide a constant drain current. Programming of the FET bias stage arrangement. The operating current of each FET group is achieved by resistors connected to the R_{CAL1} and R_{CAL2} pins. It is allowing input FETs to be biased for optimum noise, amplifier FETs for optimum gain. Amplifier FETs can be operated at currents in the range 4 to 15mA. D1 and D3 can be programmed with R_{CAL1} over the range of 4 to 15mA. D2 and D4 are programmed with R_{CAL2}.

Drain voltages of amplifier stages are set at 2.0V and are current limited to approximately current set by their associated R_{CAL} resistors.

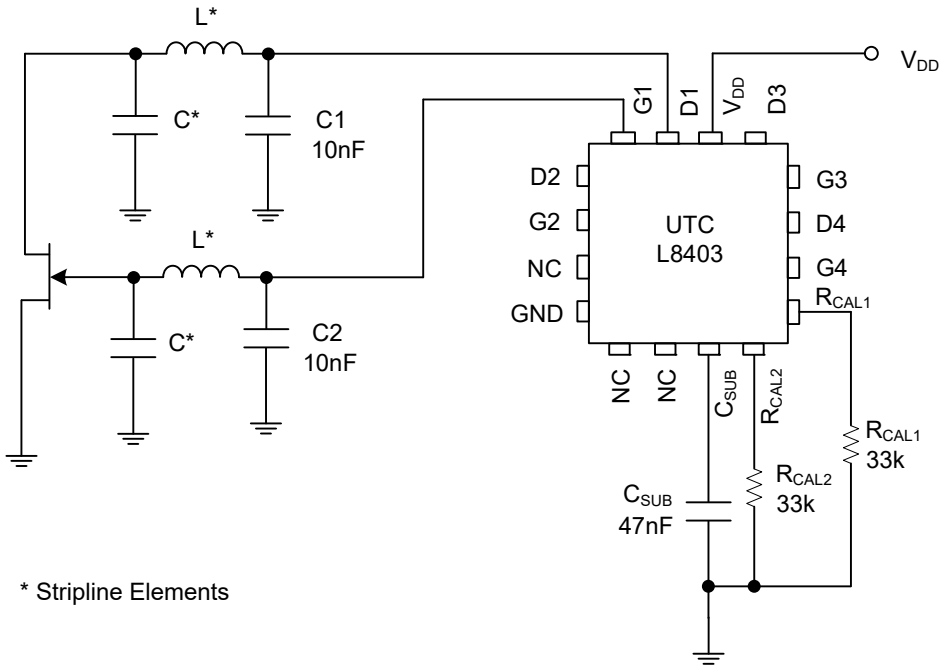
Depletion mode FETs require a negative voltage bias supply when operated in grounded source circuits. The UTC **L8403** includes an integrated switched capacitor DC-DC converter generating a regulated output of -2V to allow single supply operation. The UTC **L8403** has been designed to be used with supply rails of 2.1V to 5.5V and the V_{DD} range has been extended to 5.5V to allow for 10% supply variation.

It is possible to use less than the full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

To protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed -2.5V. Additionally each stage has its own individual current limiter. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will be limited, avoiding excessive current flow.

Device operating temperature is -40°C to +105°C to suit a wide range of environmental conditions.

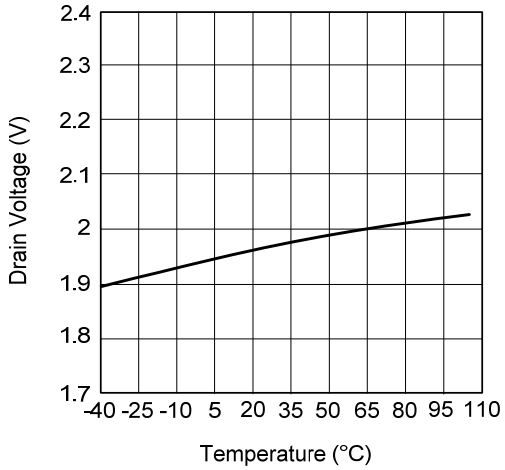
■ TYPICAL APPLICATION CIRCUIT



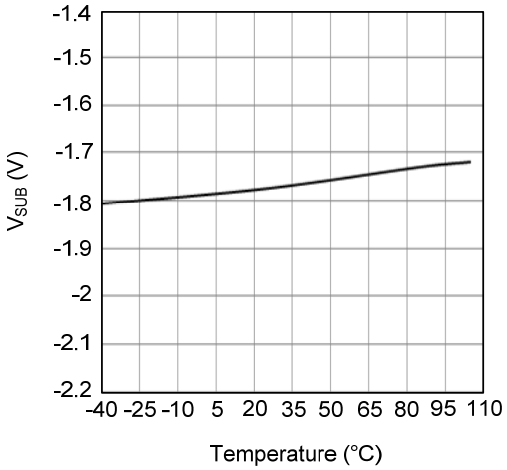
■ TYPICAL CHARACTERISTICS

(T_A=25°C, V_{DD}=2.3V, R_{CAL1}=R_{CAL2}=33kΩ (setting I_D to 10mA), unless otherwise specified.)

Drain Voltage vs. temperature



V_{SUB} vs. temperature



Drain Current vs. R_{CAL}