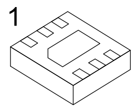
UNISONIC TECHNOLOGIES CO., LTD

BATTERY VOLTAGE AND CURRENT PROTECTION IC



DFN1616-6

■ DESCRIPTION

UTC **UB3860** is a battery protection ICs featured for accurately monitoring Li-ion or Li-Polymer battery voltage and current when charging and discharging the batteries. When over charge, over discharge and short circuit conditions happened, UTC **UB3860** battery protection ICs will control the charging or discharging output pins to control charge or discharge MOSFETs to cut off the charging or discharging path accordingly to protect the batteries from being damaged.

UTC **UB3860** battery protection ICs monitor the charge/discharge/short circuit current by external current sensing resistor, to provide very precise current sensing control.

UTC **UB3860** battery protection IC embeds with high ESD protection circuit to prevent from ESD issues in mass production and in use.

UTC **UB3860** battery protection IC power consumption when normal operation is low. For power saving, UTC **UB3860** battery protection IC provides 2 power saving modes: Standby mode and Power Down mode.

■ FEATURES

* Voltage detection and release
  Overcharge Detection Voltage
  Overcharge Release Voltage
  Overdischarge Detection Voltage
  Overdischarge Release Voltage
* Current detection and release
  Discharge Overcurrent Detection Voltage
  Charge Overcurrent Detection Voltage
  Load Short-Circuit Detection Voltage
* 0V Battery Charge Inhibition Battery Voltage
* Operation Modes
  Normal Mode: 2.5uA (Typ.), 4.0uA (Max.)
  Standby Mode: 1.0uA (Typ.), 1.5uA (Max.)
  Power Down Mode: 0.1uA (Max.)

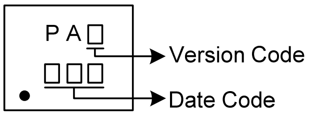
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UB3860L-xx-K06-1616-R	UB3860G-xx-K06-1616-R	DFN1616-6	Tape Reel

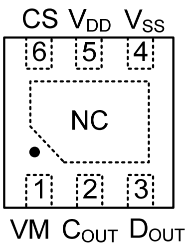
Note: xx: Serial Code, refer PRODUCT LINE UP

UB3860G-xx-K06-1616-R	
(1) Packing Type	(1) R: Tape Reel
(2) Package Type	(2) K06-1616: DFN1616-6
(3) Serial Code 2	(3) x: Refer to Delay Times
(4) Serial Code 1	(4) x: Refer to Enable/Disable and Detection / Release
(5) Green Package	(4) G : Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



DFN1616-6
(TOP VIEW)

■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	VM	Input pin for charger negative voltage.
2	C_{OUT}	Charge FET Gate Drive Output.
3	D_{OUT}	Discharge FET Gate Drive Output.
4	V_{SS}	Ground.
5	V_{DD}	Input pin for positive power supply voltage.
6	CS	Over-current detection input pin.
Exposed PAD	NC	Thermal pad.

■ PRODUCT LINE UP

Table 1. Enable/Disable and Detection / Release

CODE 1	0V Battery Charge Inhibition Battery Voltage Enable/Disable	0V Battery Charge Permission Battery Voltage Enable/Disable	Overcharge Release Voltage Latch Enable/Disable	Overcharge Release Voltage Hysteresis Enable/Disable	Power Down Mode Enable/Disable	Overcharge Detection Voltage	Overcharge Release Voltage	Overdischarge Detection Voltage	Overdischarge Release Voltage	Discharge Overcurrent Detection Voltage	Charge Overcurrent Detection Voltage	Load Short Circuit Detection Voltage	0V Battery Charge Inhibition Battery Voltage	0V Battery Charge Permission Battery Voltage	Delay Times
	V_{0INH}	V_{0CHG}	$V_{det1RelEN}$	$V_{det1RelHEN}$	M_{PD}	V_{det1}	$V_{det1Rel}$	V_{det2}	$V_{det2Rel}$	V_{det3}	V_{det4}	V_{Short}	V_{0INH}	V_{0CHG}	-
						V	V	V	V	mV	mV	mV	V	V	
UB3860-A	Enable	Disable	Disable	Enable	Disable	4.475	4.275	2.500	2.900	15	-15	33	0.9	--	A

Table 2. Delay Times

CODE 2	Overcharge Detection Delay Time [tV_{det1}](s)	Overcharge Release Delay Time [$tV_{det1Rel}$](ms)	Overdischarge Detection Delay Time [tV_{det2}](ms)	Overdischarge Release Delay Time [$tV_{det2Rel}$](ms)	Discharge Overcurrent Detection Delay Time [tV_{det3}](ms)	Discharge Overcurrent Release Delay Time [$tV_{det3Rel}$](ms)	Charge Overcurrent Detection Delay Time [tV_{det4}](ms)	Charge Overcurrent Release Delay Time [$tV_{det4Rel}$](ms)	Load Short Circuit Detection Delay Time [V_{Short}](μs)
A	1.0	3	32	1.5	68	6	16	4.5	250

■ ABSOLUTE MAXIMUM RATING (V_{SS}=0V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ 6	V
Negative Voltage Input	V_{VM}	V_{DD}-28 ~ V_{DD}+0.3	V
Charge FET Control	V_{COUT}	V_{DD}-28 ~ V_{DD}+0.3	V
Discharge FET Control	V_{DOUT}	-0.3 ~ V_{DD}+0.3	V
Current Sense Input	V_{CS}	-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{STG}	-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{OP}		1.5		5.5	V
Operating Temperature	T_{OPR}		-40		+85	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{Normal}	I_{Normal}	V_{DD}=3.5V, V_{CS}=0V, V_{VM}=0V		2.5	4	μA
$I_{Standby}$	$I_{Standby}$	V_{DD}=1.5V, V_{CS}=0V, V_{VM}=1.5V		1	1.5	μA
I_{Power_Down}	I_{Power_Down}	V_{DD}=1.5V, V_{CS}=0V, V_{VM}=1.5V			0.1	μA
RESISTANCES						
R_{VMD} : VM pin Pull-up Resistance		V_{DD}=1.8V, V_{CS}=0V, V_{VM}=0V		312	624	kΩ
R_{VMS} : VM pin Pull-down Resistance		V_{DD}=3.5V, V_{CS}=0V, V_{VM}=1V		23	46	kΩ
R_{COH} : C_{OUT} pin Pull-up Resistance		V_{DD}=3.5V, V_{CS}=0V, V_{VM}=0V, V_{COUT}=3V		4.5	9	kΩ
R_{COL} : C_{OUT} pin Pull-down Resistance		V_{DD}=4.5V, V_{CS}=0V, V_{VM}=0V, V_{COUT}=3V		3.1	6.2	kΩ
R_{DOH} : D_{OUT} pin Pull-up Resistance		V_{DD}=3.5V, V_{CS}=0V, V_{VM}=0V, V_{DOUT}=3V		1.6	3.2	kΩ
R_{DOL} : D_{OUT} pin Pull-down Resistance		V_{DD}=1.8V, V_{CS}=0V, V_{VM}=0V, V_{DOUT}=0.5V		2.1	4.2	kΩ
R_{CS} : CS pin Input Resistance		V_{DD}=3.5V, V_{CS}=0.05V, V_{VM}=0V		117	234	kΩ
0V BATTERY CHARGE PERMISSION FUNCTION						
V_{0CHG}	V_{0CHG}		0.5	0.9	1.3	V
0V BATTERY CHARGE INHIBITION FUNCTION						
V_{0INH}	V_{0INH}		0.5	0.9	1.3	V

■ BATTERY PROTECTION ACCURACY (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcharge Detection Voltage	V_{det1}		-0.015	V_{det1}	+0.015	V
Overcharge Release Voltage	$V_{det1Rel}$		-0.020	$V_{det1Rel}$	+0.020	V
Overdischarge Detection Voltage	V_{det2}		-0.025	V_{det2}	+0.025	V
Overdischarge Release Voltage	$V_{det2Rel}$		-0.030	$V_{det2Rel}$	+0.030	V
Discharge Overcurrent Detection Voltage	V_{det3}		-0.001	V_{det3}	+0.001	V
Discharge Overcurrent Release Voltage	$V_{det3Rel}$	Release condition: Base onVM voltage to release		$V_{det3Rel}$		V
Charge Overcurrent Detection Voltage	V_{det4}		-0.001	V_{det4}	+0.001	V
Charge Overcurrent Release Voltage	$V_{det4Rel}$	Release condition: Base onVM voltage to release		$V_{det4Rel}$		V
Load Short Circuit Detection Voltage	V_{Short}		-0.005	V_{Short}	+0.005	V
Load Short Circuit Release Voltage	V_{SCRel}	Release condition: Base onVM voltage to release		V_{SCRel}		V
0V Battery Charge Inhibition Battery Voltage	V_{0INH}		-0.400	V_{0INH}	+0.400	V
0V Battery Charge Permission Battery Voltage	V_{0CHG}		-0.400	V_{0CHG}	+0.400	V

■ BATTERY PROTECTION DETECTION DELAY TIME ACCURACY

(T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcharge Detection Delay Time	tV_{det1}		-30%	tV_{det1}	+30%	s
Overcharge Release Delay Time	$tV_{det1Rel}$		-30%	$tV_{det1Rel}$	+30%	ms
Overdischarge Detection Delay Time	tV_{det2}		-30%	tV_{det2}	+30%	ms
Overdischarge Release Delay Time	$tV_{det2Rel}$		-30%	$tV_{det2Rel}$	+30%	ms
Discharge Overcurrent Detection Delay Time	tV_{det3}		-30%	tV_{det3}	+30%	ms
Discharge Overcurrent Release Delay Time	$tV_{det3Rel}$		-30%	$tV_{det3Rel}$	+30%	ms
Charge Overcurrent Detection Delay Time	tV_{det4}		-30%	tV_{det4}	+30%	ms
Charge Overcurrent Release Delay Time	$tV_{det4Rel}$		-30%	$tV_{det4Rel}$	+30%	ms
Load Short Circuit Detection Delay Time	tV_{Short}		-50%	tV_{Short}	+50%	us

■ DESCRIPTION OF OPERATION

Based on different test items, the test circuits are different and shown as below. C_{OUT} pin and D_{OUT} pin are used as control pins to turn on or turn off the external charge and discharge MOSFETs. When C_{OUT} pin or D_{OUT} pin is output "L", the external MOSFET is turned off. The charge or discharge paths are cut off. At this time, charging or discharging the battery is not allowed. When the abnormal situation is released, the C_{OUT} pin or D_{OUT} pin will output "H" to turn on the MOSFET to allow the battery to be charged or discharged.

Initially, the C_{OUT} and D_{OUT} pins are output "H" to ensure the battery can be charged or discharged. V_{DD} pin in the test circuit can be treated as battery voltage.

Overcharge Detection and Release

The overcharge detection voltage is measured by the test circuit 1 and shown as below.

Test steps：

1. Set V_{DD} voltage to 3.60V and CS to 0V.
2. Increase V_{DD} voltage gradually.
3. When the voltage on V_{DD} is increased, exceeds the Vdet1 detection voltage and the detection delay time (tV_{det1}) expired, C_{OUT} pin will transition from "H" to "L".
4. At this moment, enter the charging overvoltage protection state.
5. Then test charging overvoltage release measurement.
6. Decrease V_{DD} voltage gradually.
7. When the voltage on V_{DD} changes and is lower than $V_{det1Rel}$ and the delay time expired $tV_{det1Rel}$, C_{OUT} pin will transition from "L" to "H".
8. There are two conditions as below.

(1) System connects load：

When the battery voltage is lower than V_{det1} and VM pin voltage is higher than 0.25V(typical) and the delay time expired $tV_{det1Rel}$, overcharge condition is released.

(2) Charger remove：

When the battery voltage is lower than $V_{det1Rel}$ and VM pin voltage is lower than 0.25V(typical) and the delay time expired $tV_{det1Rel}$, overcharge condition is released

Overdischarge Detection and Release

The overdischarge detection voltage is measured by the test circuit 2 and shown as below.

Test steps：

1. Set V_{DD} voltage to 3.60V and CS=VM to 0V.
2. Decrease V_{DD} voltage gradually
3. When the voltage on V_{DD} is decreased, goes lower than the V_{det2} detection voltage and the detection delay time (tV_{det2}) expired, D_{OUT} pin will transition from "H" to "L".
4. At this moment, enter the discharge overvoltage protection state
5. Then test discharge overvoltage release measurement
6. Increase V_{DD} voltage gradually
7. When the voltage on V_{DD} changes and goes higher than $V_{det2Rel}$ and the delay time expired $tV_{det2Rel}$, D_{OUT} pin will transition from "L" to "H".
8. At this moment, the discharge overvoltage protection state is released.

■ DESCRIPTION OF OPERATION (Cont.)

Discharge Over Current Detection and Release

The discharge over current detection is measured by the test circuit 2 and shown as below.

Test steps：

1. Set V_{DD} voltage to 3.60V and CS=VM to 0V.
2. Increase CS voltage gradually.
3. When the voltage on CS pin is increased and the voltage V_{CS} is higher than V_{SS} plus V_{det3} and the detection delay time (tV_{det3}) expired, D_{OUT} pin will transition from "H" to "L".
4. At this moment, enter the discharge overcurrent protection state
5. Then test discharge overcurrent release measurement
6. Decrease VM voltage gradually
7. For release condition：When the VM pin voltage is lower than 0.25V (typical) and the delay time expired tV_{det3}.
8. Discharge over current condition is released.
9. The relation between VM and Rload is shown as following :

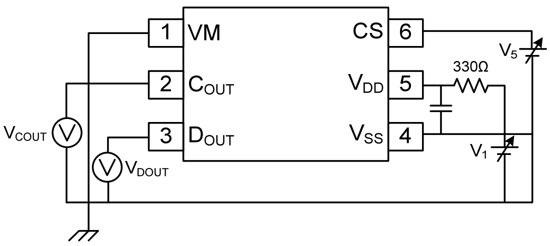
$$V_{VM}=V_{DD} \times R_{VMS} / (R_{VMS}+Rload)$$

Charge Over Current Detection and Release

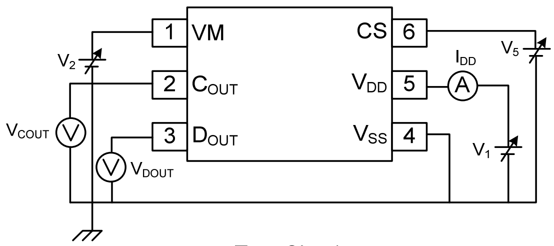
The charge over current detection is measured by the test circuit 2 and shown as below.

Test steps：

1. Set V_{DD} voltage to 3.60V and CS=VM to 0V.
2. Decrease CS voltage gradually
3. When the voltage on CS pin is decreased and the voltage V_{CS} is lower than V_{SS} plus Vdet4 and the detection delay time (tV_{det4}) expired, C_{OUT} pin will transition from "H" to "L".
4. At this moment, enter the charging overcurrent protection state
5. Then test charging overcurrent release measurement
6. Increase VM voltage gradually
7. For release condition：When the charger is removed, the system connects load, VM pin voltage is higher than 0.25V (typical) and the delay time expired tV_{det4}
8. Charge over current condition is released.



Test Circuit 1



Test Circuit 2

■ DESCRIPTION OF OPERATION (Cont.)

Load Short Circuit Detection and Release

The load short circuit detection is measured by the test circuit 2 and shown as below.

Test steps：

1. Set V_{DD} voltage to 3.60V and CS=VM to 0V
2. Increase CS voltage gradually
3. When the voltage on CS pin is increased and the voltage V_{CS} is higher than V_{SS} plus V_{short}, before the detection delay time (tV_{det3}) is expired, the voltage V_{CS} keeps on increase to be higher than V_{SS} plus V_{short} and the detection delay time (tV_{short}) expired, D_{OUT} pin will transition from "H" to "L".
4. At this moment, enter the short-circuit over-current protection state
5. Then test short-circuit over-current release measurement
6. Decrease VM voltage gradually.
7. When the VM pin voltage is lower than 0.25V (typical) and the delay time expired tV_{short}, D_{OUT} pin will transition from "L" to "H".
8. Load short circuit condition is released.
9. The relation between VM and Rload is shown as following :

$$V_{VM}=V_{DD} \times R_{VMS}/(R_{VMS}+Rload)$$

Power Consumption in Normal Operation Mode

The normal mode power consumption is measured by the test circuit 2 and shown as below.

Test steps：

1. Set V_{DD} =3.50V
2. Set V_{CS}=V_{VM}=0V
3. C_{OUT} and D_{OUT} floating
4. Then measure the current I_{normal} going into V_{DD} pin.
5. Get the power consumption of normal mode I_{normal}

Power Consumption in Standby Mode

The standby mode power consumption is measured by the test circuit 2 and shown as below.

Test steps：

1. Set V_{DD}=V_{VM}=1.50V
2. Set V_{CS}=0V
3. C_{OUT} and D_{OUT} floating
4. Then measure the current $I_{standby}$ going into V_{DD} pin.
5. Get The power consumption of standby mode $I_{standby}$.

Pull-Up Resistance between V_{DD} to VM pin (R_{VMD})

The pull-up resistance between V_{DD} and VM pin is measured by the test circuit 3 and shown as below.

Test steps：

1. Set V_{DD}=1.80V
2. Set V_{CS}=V_{VM}=0V
3. C_{OUT} and D_{OUT} floating
4. Then measure the current I_{VM}.
5. The pull-up resistance between V_{DD} and VM pin is obtained by the relation：

$$R_{VMD}=V_{DD} / I_{VM}$$

■ DESCRIPTION OF OPERATION (Cont.)

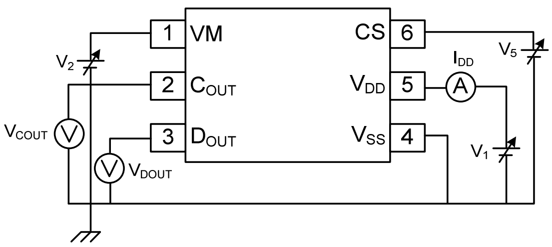
Pull-Down Resistance between VM to V_{DD} pin (R_{VMS})

The pull-down resistance between V_{DD} and VM pin is measured by the test circuit 3 and shown as below.

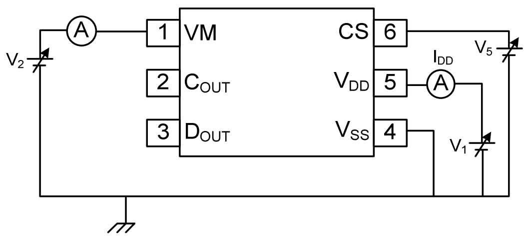
Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=0V
3. Set VM=1.0V
4. C_{OUT} and D_{OUT} floating
5. Then measure the current I_{VM}.
6. The pull-down resistance between V_{DD} and VM pin is obtained by the relation：

$$R_{VMS}=V_{VM} / I_{VM}$$



Test Circuit 2



Test Circuit 3

C_{OUT} pin Pull-up Resistance (R_{COH})

The pull-up resistance on C_{OUT} pin is measured by the test circuit 4 and shown as below.

Test steps：

1. Set V_{DD}=3.50V,
2. Set V_{CS}=V_{VM}=0V
3. Set V_{COUT}=3.0V
4. D_{OUT} floating, then measure the current I_{COUT}.
5. The C_{OUT} pin pull-up resistance is obtained by the relation：

$$R_{COH}=(V_{DD}-V_{COUT}) / I_{COUT}$$

C_{OUT} pin Pull-down Resistance (R_{COL})

The pull-down resistance on C_{OUT} pin is measured by the test circuit 4 and shown as below.

Test steps：

1. Set V_{DD}=4.50V
2. Set V_{CS}=V_{VM}=0V
3. Set V_{COUT}=3.0V
4. D_{OUT} floating
5. Then measure the current I_{COUT}.
6. The C_{OUT} pin pull-down resistance is obtained by the relation：

$$R_{COL}=V_{COUT} / I_{COUT}$$

D_{OUT} pin Pull-up Resistance (R_{DOH})

The pull-up resistance on D_{OUT} pin is measured by the test circuit 4 and shown as below.

Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=V_{VM}=0V
3. Set V_{DOUT}=3.0V
4. C_{OUT} floating
5. Then measure the current I_{DOUT}.
6. The D_{OUT} pin pull-up resistance is obtained by the relation：

$$R_{DOH}=(V_{DD}-V_{DOUT}) / I_{DOUT}$$

■ DESCRIPTION OF OPERATION (Cont.)

D_{OUT} pin Pull-Down Resistance (R_{DOL})

The pull-down resistance on D_{OUT} pin is measured by the test circuit 4 and shown as below.

Test steps：

1. Set V_{DD}=1.80V
2. Set V_{CS}=V_{VM}=0V
3. Set V_{DOUT}=0.50V
4. C_{OUT} floating
5. Then measure the current I_{DOUT}.
6. The D_{OUT} pin pull-down resistance is obtained by the relation：

$$R_{DOL}=V_{DOUT} / I_{DOUT}$$

CS pin Input Resistance (R_{CS})

The input resistance on CS pin is measured by the test circuit 4 and shown as below.

Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=0.05V
3. Set V_{VM}=0V
4. C_{OUT} and D_{OUT} floating
5. Then measure the current I_{CS}.
6. The CS pin input resistance is obtained by the relation：

$$R_{CS}=V_{CS} / I_{CS}$$

0V Battery Charge Inhibition Voltage (V_{0INH})

The 0V battery charge inhibition voltage threshold is measured by the test circuit 2 and shown as below.

Test steps：

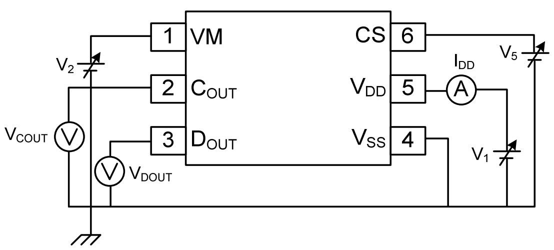
1. Set V_{DD}=V_{CS}=0V
2. Set V_{VM}=-4.0V
3. D_{OUT} floating.
4. Increase V_{DD} voltage gradually, monitor V_{COUT}.
5. The V_{0INH} equals to the V_{DD} once V_{COUT}>=V_{VM}+0.10V.

0V Battery Charge Permission Voltage (V_{0CHA})

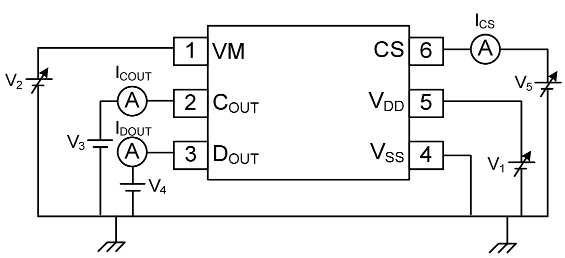
The 0V battery charge permission voltage threshold is measured by the test circuit 2 and shown as below.

Test steps：

1. Set V_{DD}=V_{CS}=0V
2. Set V_{VM}=0V
3. D_{OUT} floating.
4. Decrease VM voltage gradually, monitor V_{COUT}.
5. The V_{0CHA} equals to the ｜VM｜ once V_{COUT}>=V_{VM}+0.10V



Test Circuit 2



Test Circuit 4

■ DESCRIPTION OF OPERATION (Cont.)

Overcharge Detection Delay Time (tV_{det1})

The overcharge detection delay time is measured by the test circuit 5 and shown as below.

Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=V_{VM}=0V
3. D_{OUT} floating
4. Then monitor C_{OUT} pin transition from "H" to "L".
5. Increase the V_{DD} voltage. When V_{DD} voltage exceeds the V_{det1} detection threshold, the internal delay time counter starts to count. When the internal delay time counts exceeds the tV_{det1}, C_{OUT} pin will transition from "H" to "L".
6. tV_{det1} equals to the time period between V_{DD} voltage exceeds Vdet1 and C_{OUT} transitions from "H" to "L".

Overdischarge Detection Delay Time (tV_{det2})

The overdischarge detection delay time is measured by the test circuit 5 and shown as below.

Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=V_{VM}=0V
3. C_{OUT} floating
4. Then monitor D_{OUT} pin transition from "H" to "L".
5. Decrease the V_{DD} voltage. When V_{DD} voltage goes lower than the V_{det2} detection threshold, the internal delay time counter starts to count. When the internal delay time counts exceeds the tV_{det2}, D_{OUT} pin will transition from "H" to "L".
6. tV_{det2} equals to the time period between V_{DD} voltage goes lower than V_{det2} and D_{OUT} transitions from "H" to "L".

Discharge Overcurrent Detection Delay Time (tV_{det3})

The discharge overcurrent detection delay time is measured by the test circuit 5 and shown as below.

Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=V_{VM}=0V
3. C_{OUT} floating
4. Then monitor D_{OUT} pin transition from "H" to "L".
5. Increase the V_{CS} voltage. When V_{CS} voltage exceeds the V_{det3} detection threshold, the internal delay time counter starts to count. When the internal delay time counts exceeds the tV_{det3}, D_{OUT} pin will transition from "H" to "L".
6. tV_{det3} equals to the time period between V_{CS} voltage exceeds V_{det3} and D_{OUT} transitions from "H" to "L".

Charge Overcurrent Detection Delay Time (tV_{det4})

The charge overcurrent detection delay time is measured by the test circuit 5 and shown as below.

Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=V_{VM}=0V
3. D_{OUT} floating
4. Then monitor C_{OUT} pin transition from "H" to "L".
5. Decrease the V_{CS} voltage. When V_{CS} voltage goes lower than the V_{det4} detection threshold, the internal delay time counter starts to count. When the internal delay time counts exceeds the tV_{det4}, C_{OUT} pin will transition from "H" to "L".
6. tV_{det4} equals to the time period between V_{CS} voltage goes lower than V_{det4} and C_{OUT} transitions from "H" to "L".

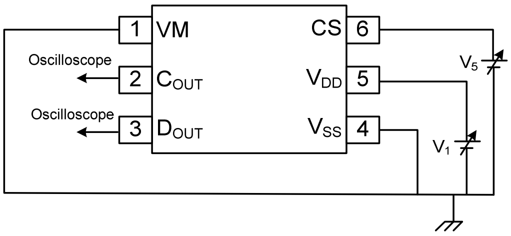
■ DESCRIPTION OF OPERATION (Cont.)

Load Short Circuit Detection Delay Time (tV_{short})

The load short circuit detection delay time is measured by the test circuit 5 and shown as below.

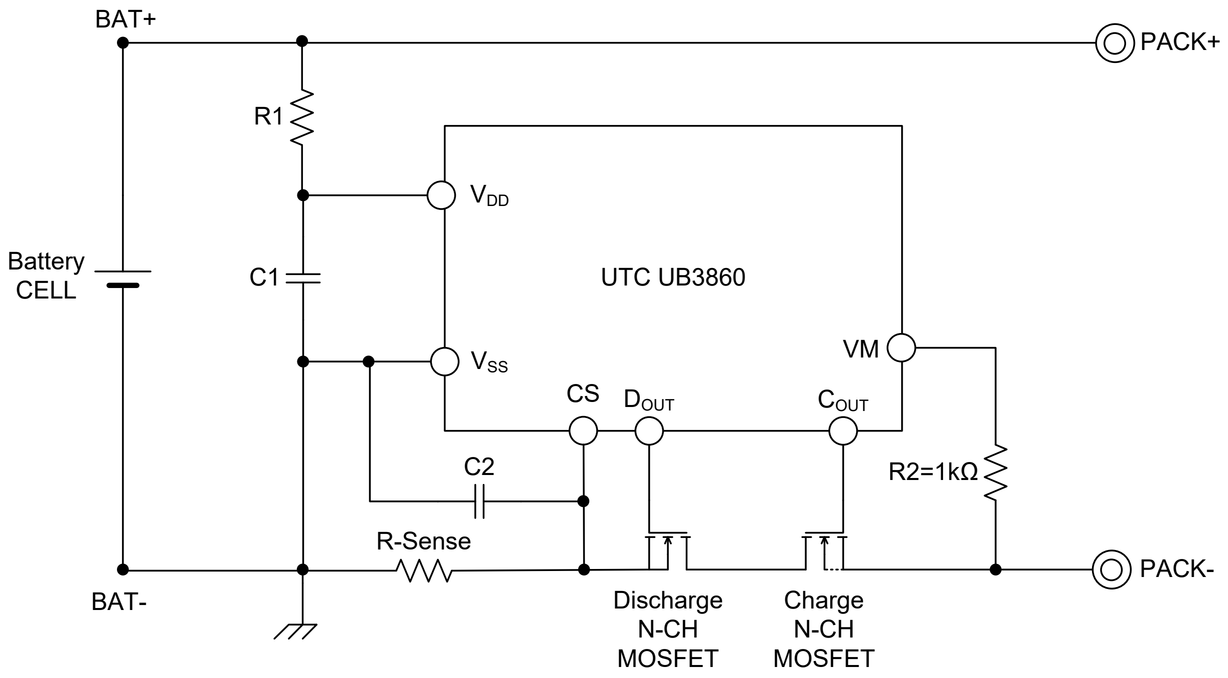
Test steps：

1. Set V_{DD}=3.50V
2. Set V_{CS}=V_{VM}=0V
3. C_{OUT} floating
4. Then monitor D_{OUT} pin transition from "H" to "L".
5. Increase the V_{CS} voltage. When V_{CS} voltage exceeds the V_{short} detection threshold, the internal delay time counter starts to count. When the internal delay time counts exceeds the tV_{short}, D_{OUT} pin will transition from "H" to "L".
6. tV_{short} equals to the time period between V_{CS} voltage exceeds V_{short} and D_{OUT} transitions from "H" to "L"



Test Circuit 5

■ TYPICAL APPLICATION CIRCUIT



BOM

Reference	MIN	TYP	MAX	UNIT	PURPOSE
R1		100	1k	Ω	
R2		1k	10k	Ω	For current limit of charger reverse connection
R-Sense					
C1	0.01	0.1	1	µF	For Input Voltage Stability
C2		0.1		µF	For Noise Suppression