



UFB4321

POWER MOSFET

80A, 150V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

DESCRIPTION

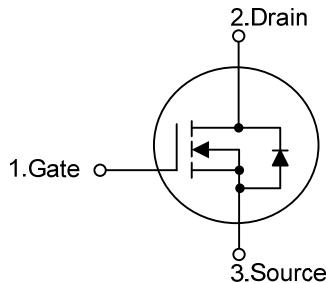
The UTC **UFB4321** is an N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low voltage inverter applications.

The UTC **UFB4321** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

- * $R_{DS(ON)} \leq 17 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=40\text{A}$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL

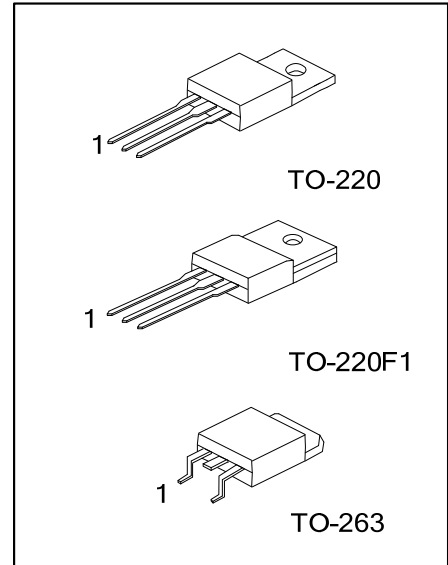


ORDERING INFORMATION

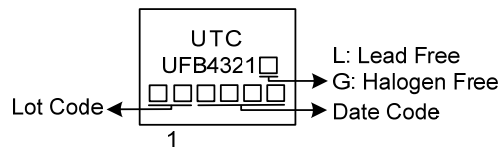
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UFB4321L-TA3-T	UFB4321G-TA3-T	TO-220	G	D	S	Tube
UFB4321L-TF1-T	UFB4321G-TF1-T	TO-220F1	G	D	S	Tube
UFB4321L-TQ2-T	UFB4321G-TQ2-T	TO-263	G	D	S	Tube
UFB4321L-TQ2-R	UFB4321G-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UFB4321G-TA3-T	(1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TF1: TO-220F1, TQ2: Tape Reel (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	150	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	80	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	120	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	224	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	17.1	V/nS
Power Dissipation	TO-220/TO-263	P_D	180	W
	TO-220F1		45	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=67\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220/TO-263	θ_{JC}	0.69	$^{\circ}\text{C}/\text{W}$
	TO-220F1		2.77	$^{\circ}\text{C}/\text{W}$

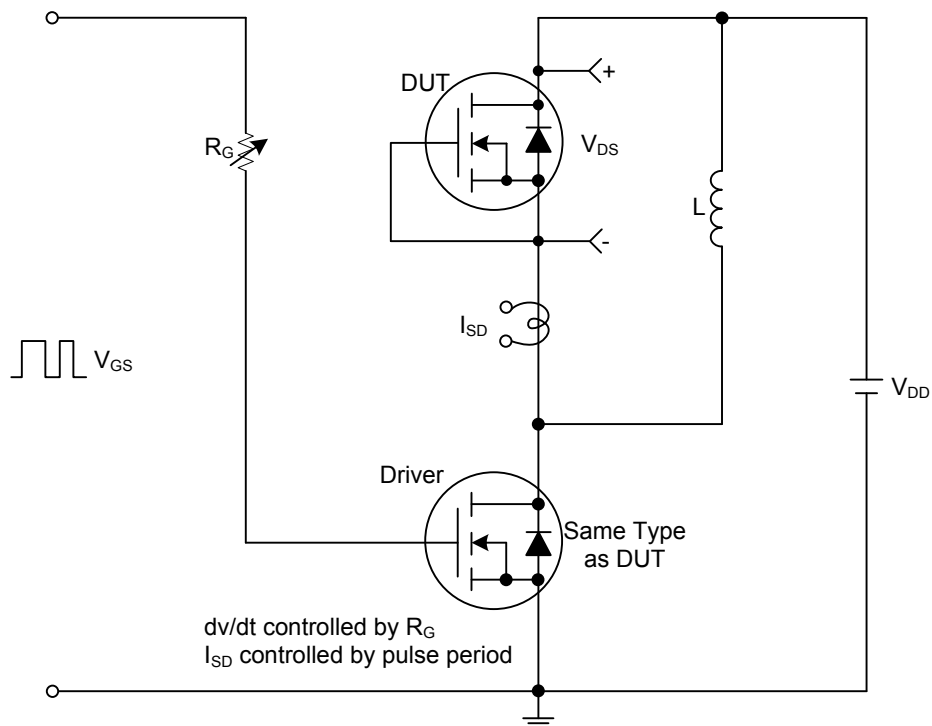
■ **ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	150			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=150V, V_{GS}=0V$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+20V, V_{DS}=0V$			+100	nA
	Reverse		$V_{GS}=-20V, V_{DS}=0V$			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$			17	m Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$		8510		pF
Output Capacitance		C_{OSS}			578		pF
Reverse Transfer Capacitance		C_{RSS}			372		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	$V_{DD}=120V, V_{GS}=10V, I_D=80A,$ (Note 1, 2)		192		nC
Gate to Source Charge		Q_{GS}			80		nC
Gate to Drain Charge		Q_{GD}			40		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	$V_{DD}=100V, V_{GS}=10V, I_D=80A,$ $R_G=3\Omega$ (Note 1, 2)		30		ns
Rise Time		t_R			27		ns
Turn-off Delay Time		$t_{D(OFF)}$			74		ns
Fall-Time		t_F			35		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=30A, V_{GS}=0V$			2.0	V
Reverse Recovery Time (Note 1)		t_{rr}	$I_S=30A, V_{GS}=0V,$		140		nS
Reverse Recovery Charge		Q_{rr}	$dl_F/dt=100A/\mu s$		672		nC

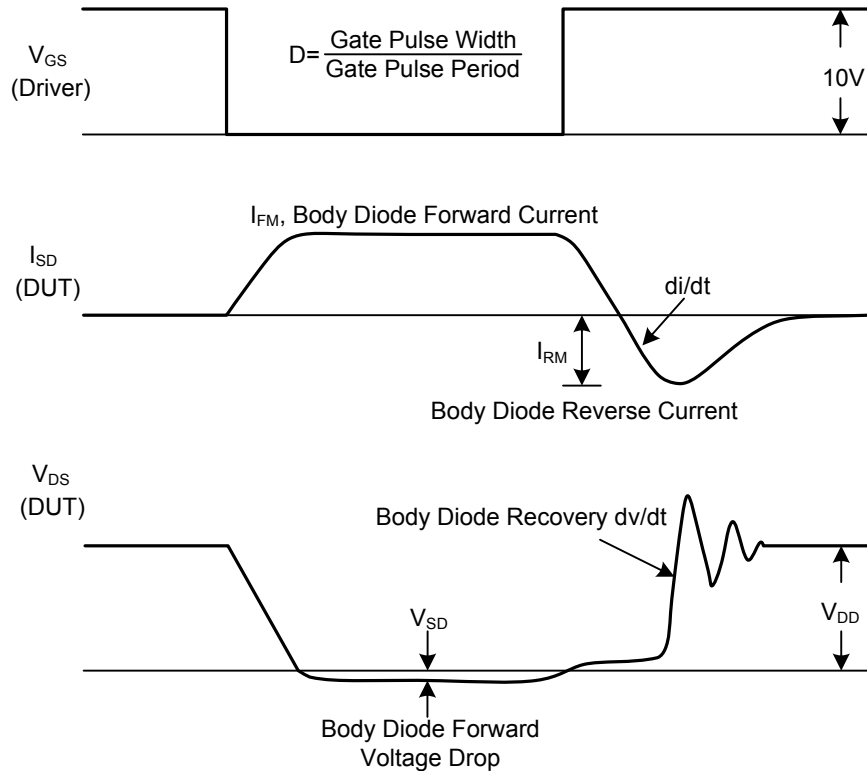
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



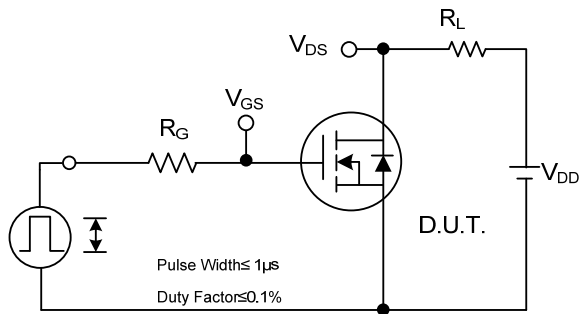
Peak Diode Recovery dv/dt Test Circuit



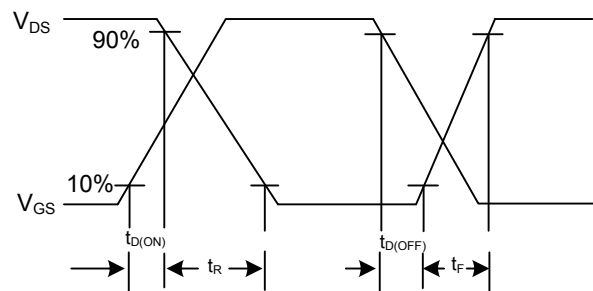
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

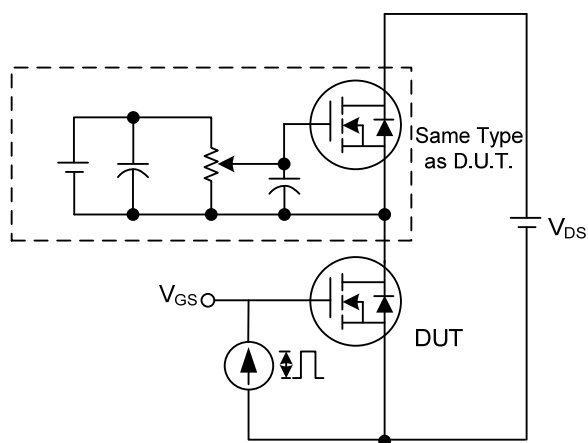
■ TEST CIRCUITS AND WAVEFORMS



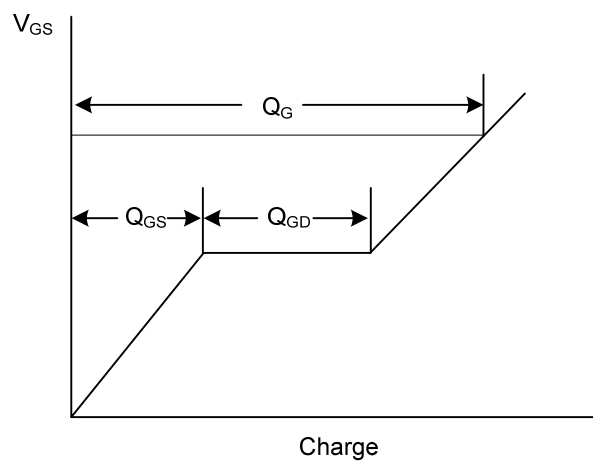
Switching Test Circuit



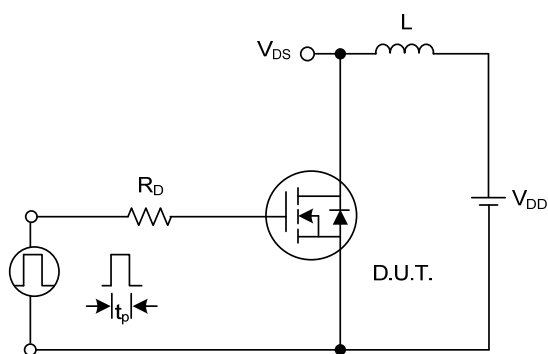
Switching Waveforms



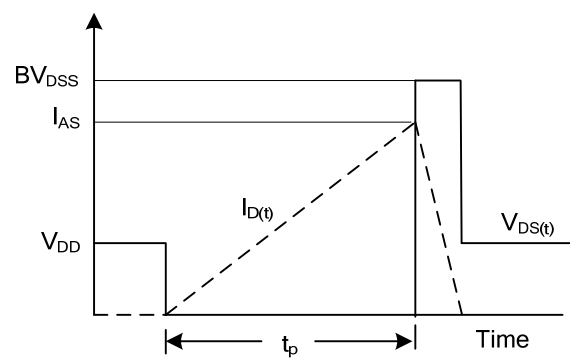
Gate Charge Test Circuit



Gate Charge Waveform

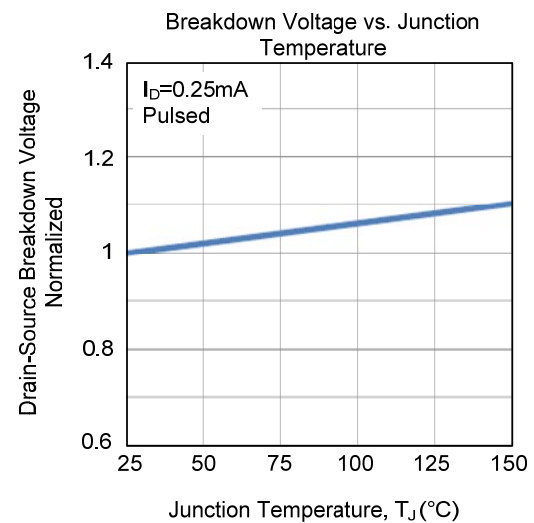
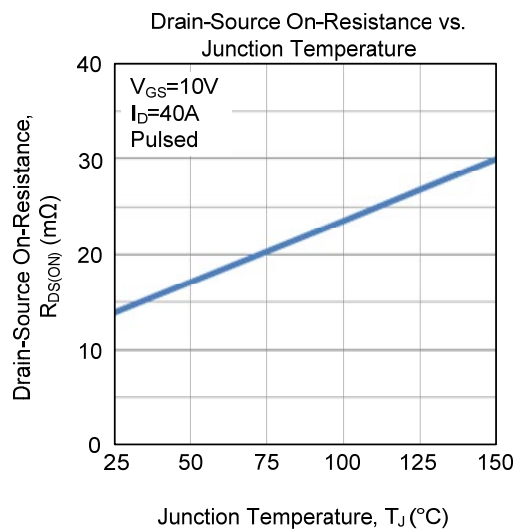
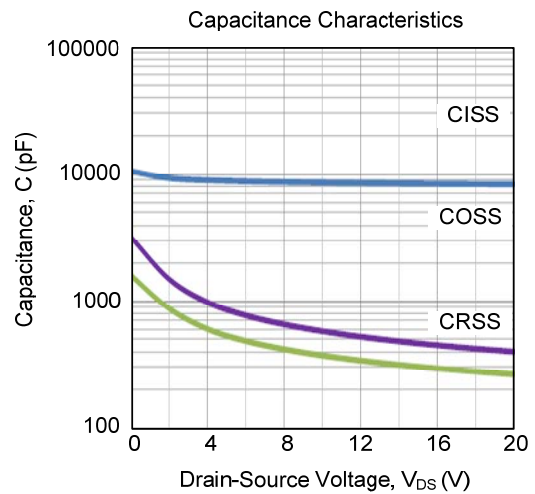
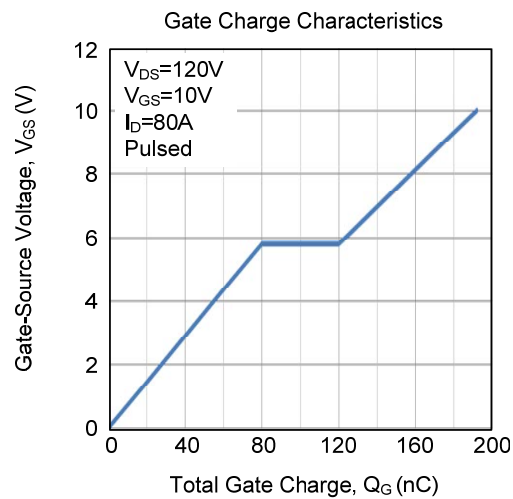
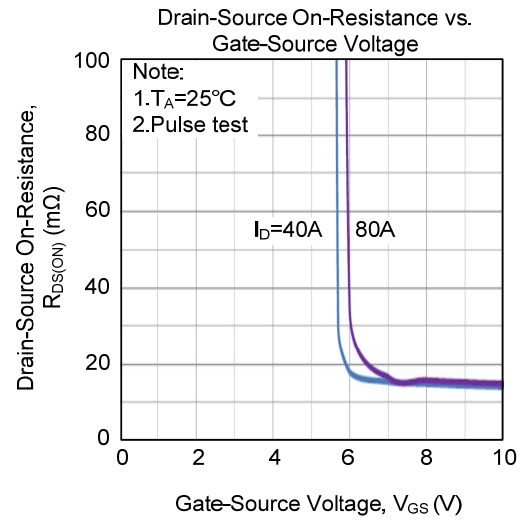
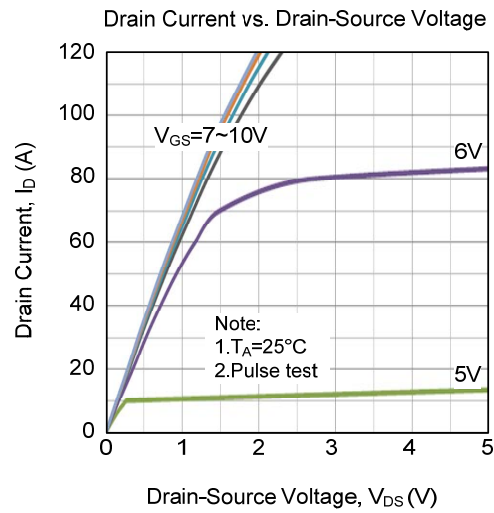


Unclamped Inductive Switching Test Circuit

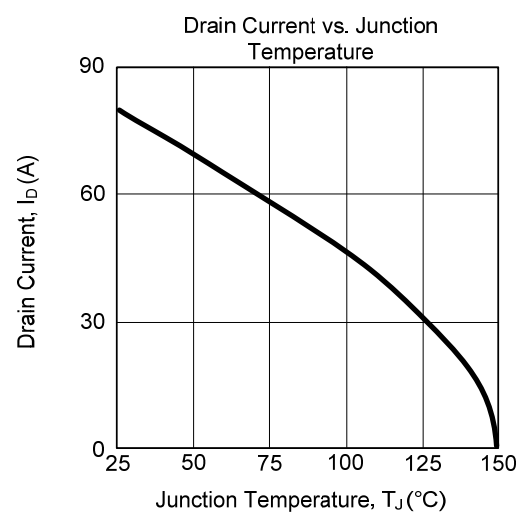
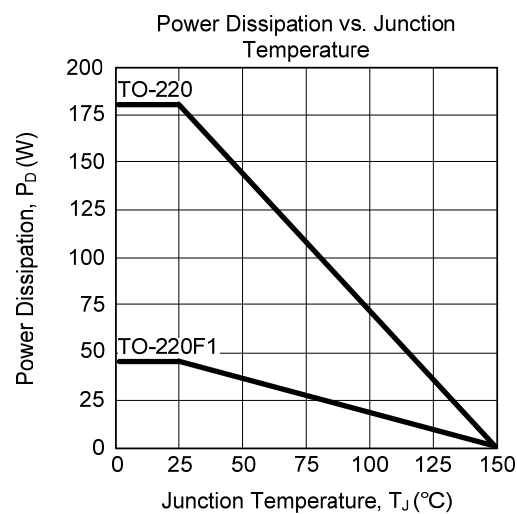
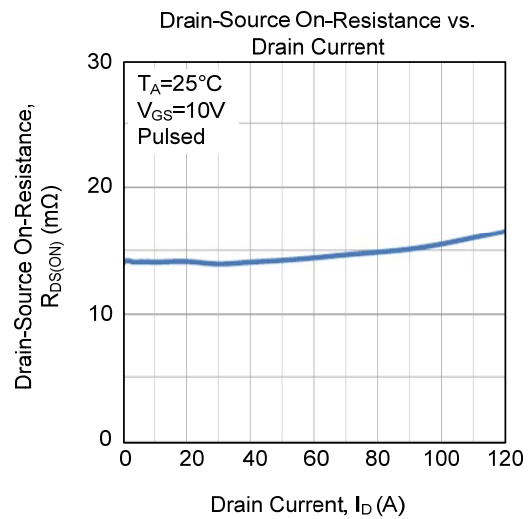
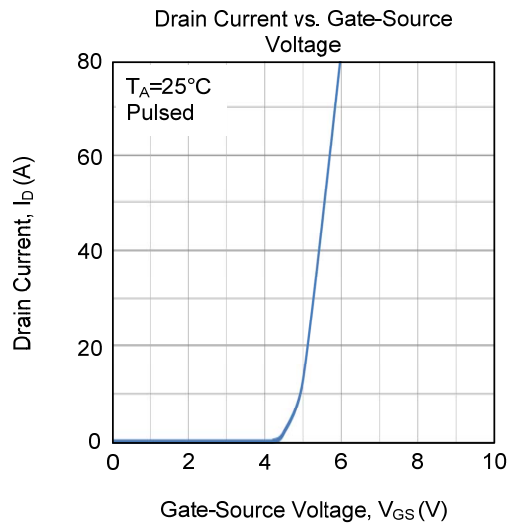
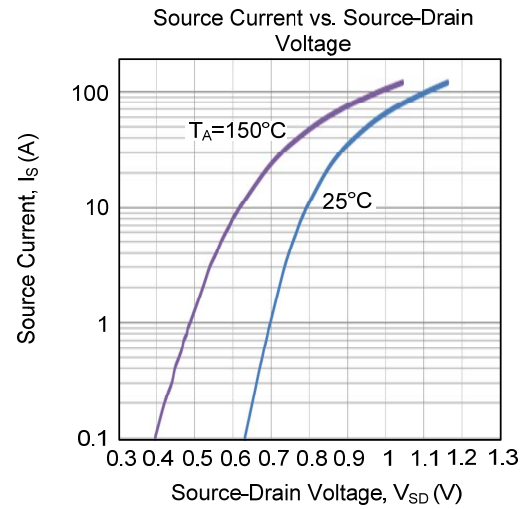
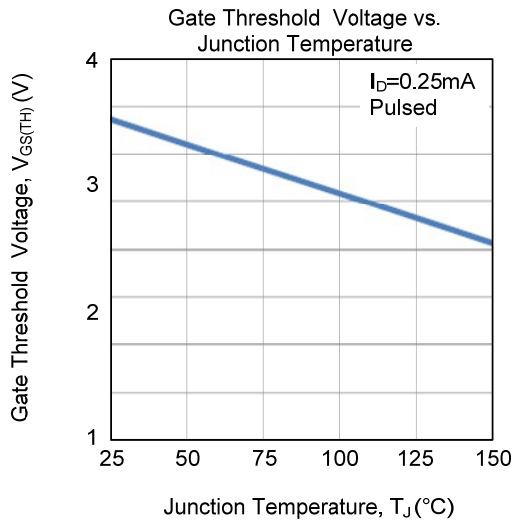


Unclamped Inductive Switching Waveforms

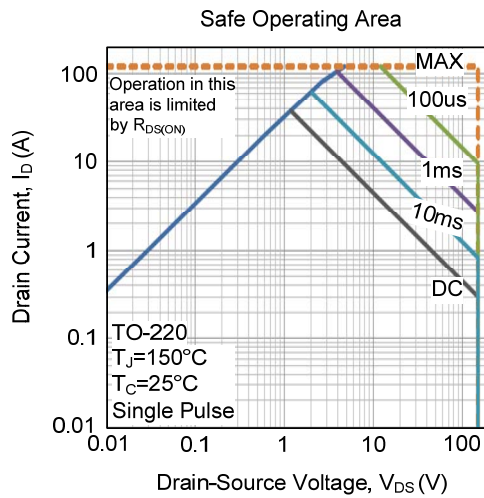
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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