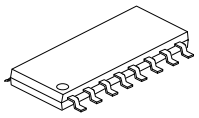
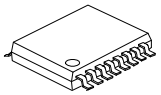
U74CBTLV3251

Preliminary ***CMOS IC***

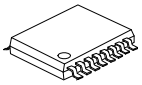
LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER



SOP-16



SSOP-16
(150mil)



TSSOP-16

■ DESCRIPTION

The **U74CBTLV3251** device is a 1-of-8 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select inputs (S0, S1, S2) control the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* 5Ω Switch Connection Between Two Ports
* Rail-to-Rail Switching on Data I/O Ports
* I_{OFF} Supports Partial-Power-Down Mode Operation

■ ORDERING INFORMATION

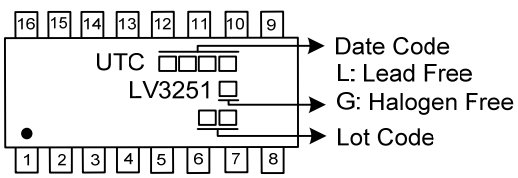
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBTLV3251L-S16-R	U74CBTLV3251G-S16-R	SOP-16	Tape Reel
U74CBTLV3251L-R16-R	U74CBTLV3251G-R16-R	SSOP-16	Tape Reel
U74CBTLV3251L-P16-R	U74CBTLV3251G-P16-R	TSSOP-16	Tape Reel

U74CBTLV3251G-S16-R

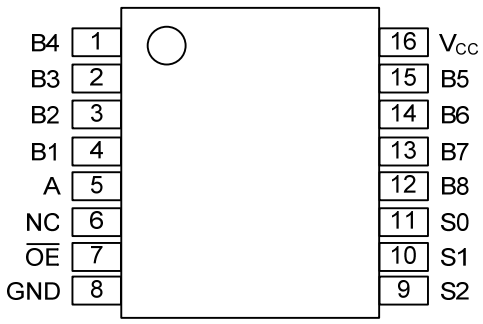
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S16: SOP-16, R16: SSOP-16, P16: TSSOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



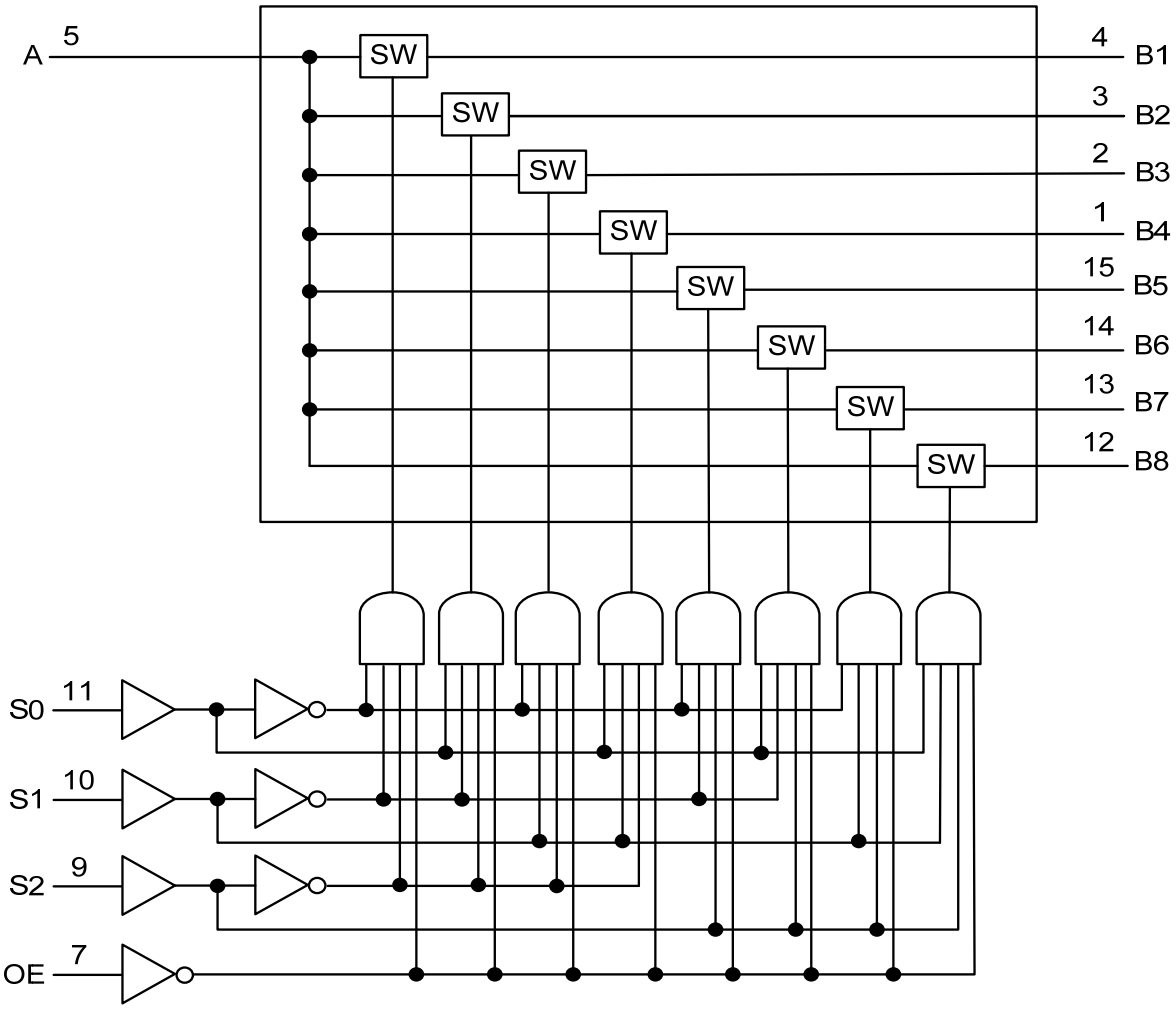
■ PIN CONFIGURATION



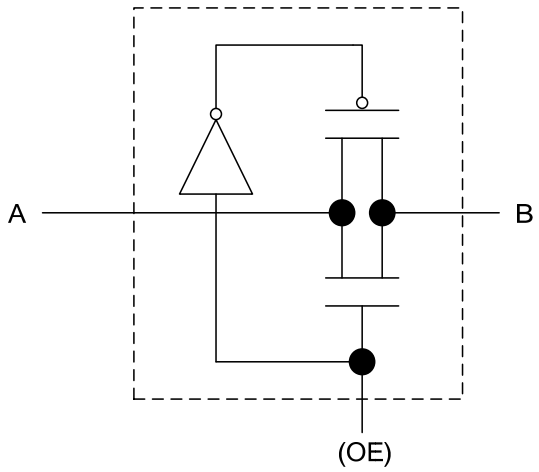
■ FUNCTION TABLE (each bus switch)

INPUTS				FUNCTION
$\overline{OE}$	S2	S1	S0	
L	L	L	L	A port = B1 port
L	L	L	H	A port = B2 port
L	L	H	L	A port = B3 port
L	L	H	H	A port = B4 port
L	H	L	L	A port = B5 port
L	H	L	H	A port = B6 port
L	H	H	L	A port = B7 port
L	H	H	H	A port = B8 port
H	X	X	X	Disconnect

■ LOGIC DIAGRAM (positive logic)



■ SIMPLIFIED SCHEMATIC (each FET switch)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 4.6	V
Input Voltage	V_{IN}		-0.5 ~ 4.6	V
Continuous Channel Through V_{CC} or GND			128	mA
Input Clamp Current	I_{IK}	V_{IO}<0	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	θ_{JA}	90	°C/W
	SSOP-16		120	°C/W
	TSSOP-16		115	°C/W

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-control input voltage	V_{IH}	V_{CC}=2.3V~2.7V	1.7			V
		V_{CC}=2.7V~3.6V	2			V
Low-control input voltage	V_{IL}	V_{CC}=2.3V~2.7V			0.7	V
		V_{CC}=2.7V~3.6V			0.8	V
Operating Temperature	T_A		-40		+125	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ ELECTRICAL CHARACTERISTICS (unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS			T_A=25°C			T_A=-40°C~+125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input Diode Voltage		V_{IK}	V_{CC} =3V, I_I=-18mA					-1.2			-1.2	V
Input Leakage Current		I_I	V_{CC}=3.6V, V_I=V_{CC} or GND					±1			±20	μA
Power off Leakage Current		I_{OFF}	V_{CC}=0, V_I or V_O=0 to 3.6V					±20			±50	μA
Quiescent Supply Current		I_{CC}	V_{CC}=3.6V, V_I= V_{CC} or GND, I_O=0					10			50	μA
Additional Quiescent Supply Current (Note 1)	Control Inputs	△I_{CC}	V_{CC}=3.6V, One input at 3V, Other inputs at V_{CC} or GND					300			2000	μA
Resistor between two ports (Note 2)		R_{ON}	V_{CC}=2.3V TYP at	V_I=0	I_I=64mA		5	8			15	Ω
					I_I=24mA		5	8			15	Ω
			V_{CC}=2.5V	V_I=1.7V	I_I=-15mA		27	40			60	Ω
			V_{CC}=3V	V_I=0V	I_I=64mA		5	7			11	Ω
					I_I=24mA		5	7			11	Ω
				V_I=2.4V	I_I=-15mA		10	15			26	Ω

Notes: 1.This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
2. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

■ SWITCHING CHARACTERISTICS

See Fig. 1 and Fig. 2 for test circuit and waveforms.

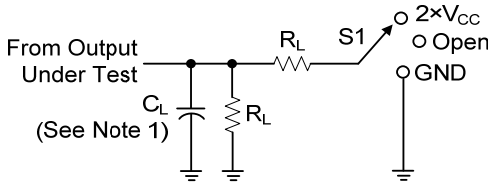
PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input (A or B) (Note) to Output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	V_{CC}=2.5V±0.2V			0.15			0.3	ns
		V_{CC}=3.3V±0.3V			0.25			0.5	ns
Propagation Delay From Input (S) to Output (A)		V_{CC}=2.5V±0.2V	1		6.1			8.1	ns
		V_{CC}=3.3V±0.3V	1		5.3			7.3	ns
Propagation Delay From Input (S) to Output (B)	t_{en} (t_{PZL}/t_{PZH})	V_{CC}=2.5V±0.2V	1		5.4			7.4	ns
		V_{CC}=3.3V±0.3V	1		4.8			6.8	ns
Propagation Delay From Input ($\overline{OE}$) to Output (A or B)		V_{CC}=2.5V±0.2V	1		5.2			7.2	ns
		V_{CC}=3.3V±0.3V	1		4.5			6.5	ns
Propagation Delay From Input (S) to Output (B)	t_{dis} (t_{PLZ}/t_{PHZ})	V_{CC}=2.5V±0.2V	1		4.8			6.8	ns
		V_{CC}=3.3V±0.3V	1		4.5			6.5	ns
Propagation Delay From Input ($\overline{OE}$) to Output (A or B)		V_{CC}=2.5V±0.2V	1		6.7			8.2	ns
		V_{CC}=3.3V±0.3V	1		7.2			8.8	ns

Note: The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

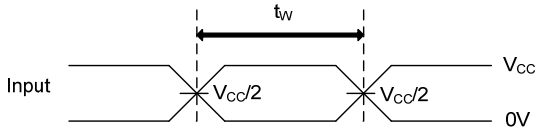
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Control input Capacitance	Control Inputs	C_I	V_O=3V or 0		3		pF
I/O Capacitance (OFF)	A Port	$C_{IO(OFF)}$	V_O=3V or 0, $\overline{OE}$ =V_{CC}		40.5		pF
	B Port				6		pF

■ TEST CIRCUIT AND WAVEFORMS

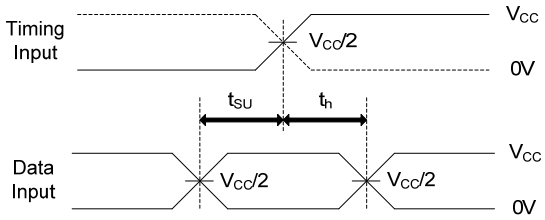


V_{CC}	C_L	R_L	VΔ
2.5V±0.2V	30pF	500Ω	0.15V
3.3V±0.3V	50pF	500Ω	0.3V

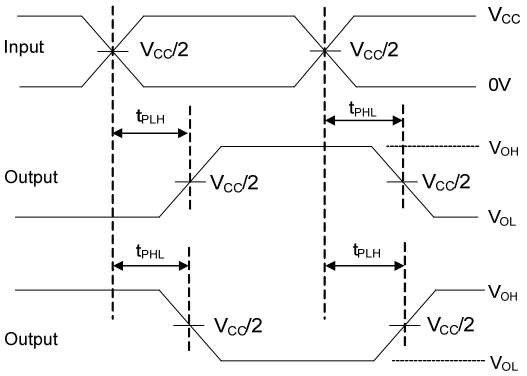
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2×Vcc
t_{PHZ}/t_{PZH}	GND



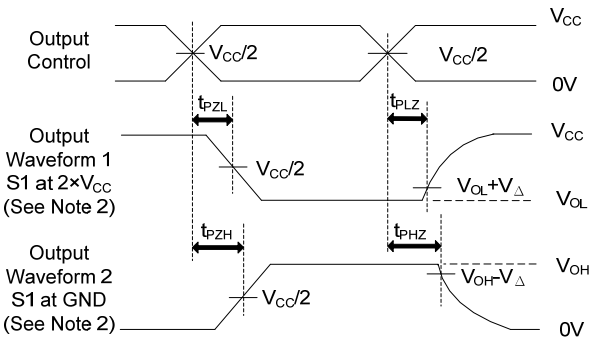
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics:
   P_{RR} ≤ 10MHz, Z_O=50Ω, t_r ≤ 2ns, t_f ≤ 2ns.
4. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
5. t_{PZL} and t_{PZH} are the same as t_{en}.
6. t_{PLH} and t_{PHL} are the same as t_{pd}.

Load circuitry and voltage waveforms