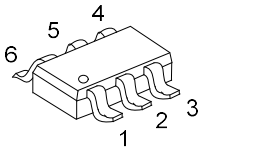
# LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS




SOT-26

## ■ DESCRIPTION

The UTC **UC3838** provides a CCM switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, and switch to power-saving mode at light load.

The UTC **UC3838** is a high performance current mode PWM controller ideally suited for low standby power. Low $V_{CC}$ startup current make the power reliable on startup design and a large value resistor could be used in the startup circuit to minimize the standby power. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition.

The UTC **UC3838** contains protection with automatic recovery including OLP (over load protection), OCP (cycle-by-cycle current limiting), and UVLO ($V_{CC}$ over voltage clamp and under voltage lockout). It also provides the protections including OTP (over temperature protection), OVP ($V_{CC}$ or DC output over voltage protection) with automatic recovery. To protect the power MOSFET, Gate-drive output is fixed up to 17V max.

The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch, which offering minima external component count in the design. Excellent EMI performance is achieved with UTC proprietary frequency hopping technique together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation.

UTC **UC3838** is packaged by using tiny SOT-26 package. It has such applications as: battery charger, power adaptor, set-top box power supplies, ink jet printers, open-frame SMPS.

## ■ FEATURES

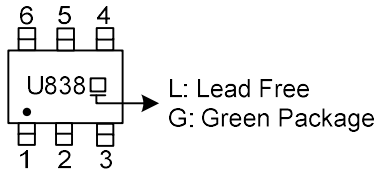
* Proprietary frequency hopping for Improved EMI performance
* Cycle-by-cycle current limiting
* CCM Power-saving mode Switching Operation
* Fixed switch frequency 65kHz TYP.
* Dynamic peak current limiting for constant output power
* Built-in synchronized slope compensation
* Gate output voltage clamped at 17V
* Adjustable DC output OVP/OTP
* OLP/$V_{CC}$ OVP/Internal OTP (automatic recovery)
* Internal Soft Start
* OTP through a NTC (latch mode)

## ■ ORDERING INFORMATION

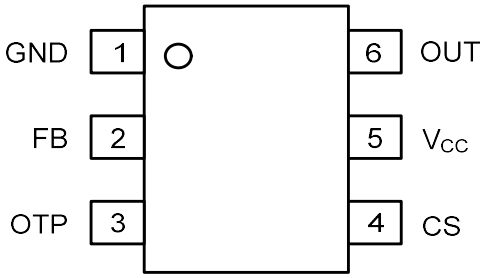
| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| UC3838L-AG6-R | UC3838G-AG6-R | SOT-26 | Tape Reel |

| | |
|---|---|
| UC3838G-AG6-R<br>(1)Packing Type<br>(2)Package Type<br>(3)Green Package | (1) R: Tape Reel<br>(2) AG6: SOT-26<br>(3) G: Halogen Free and Lead Free, L: Lead Free |

## ■ MARKING



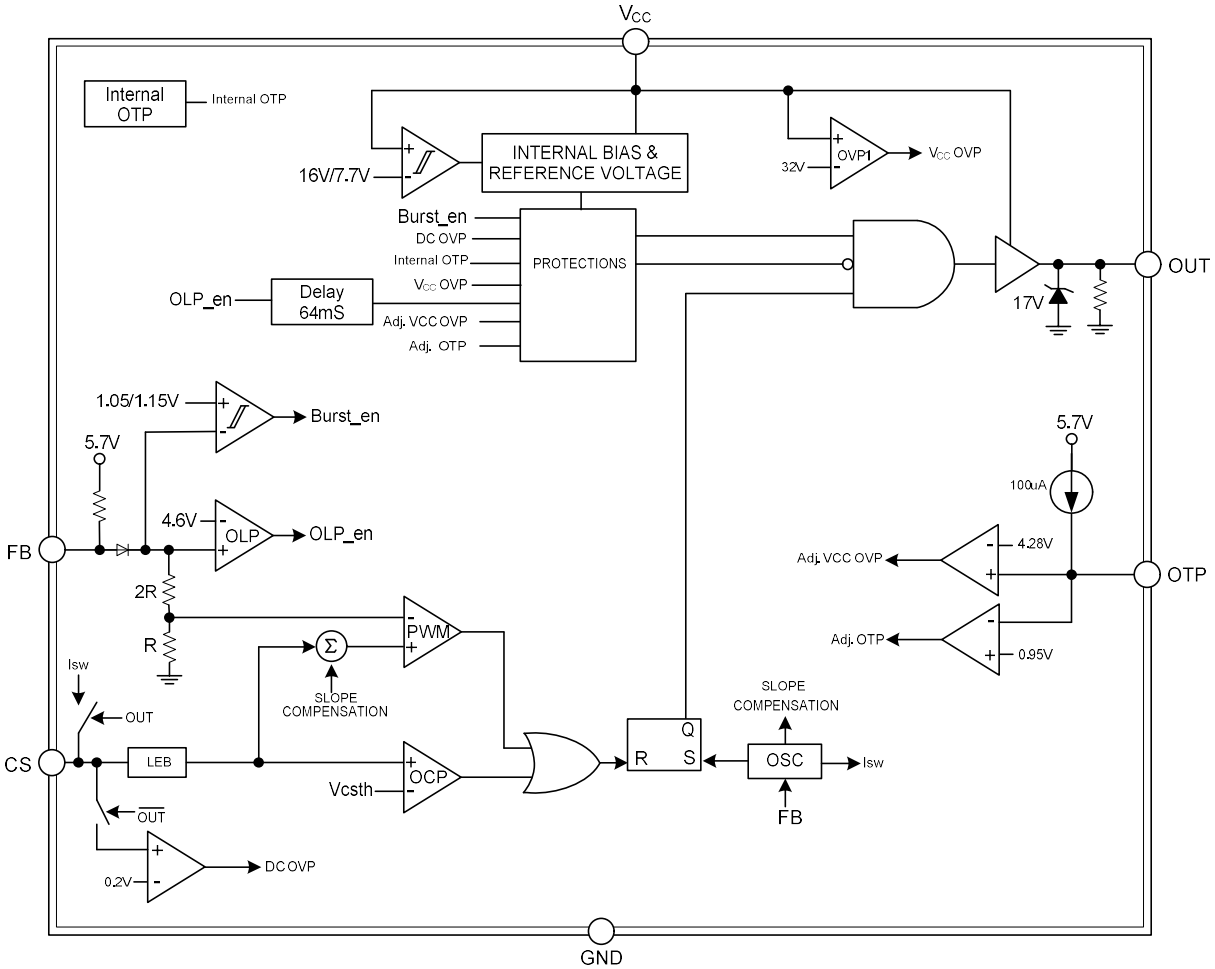
## ■ PIN CONFIGURATION




## ■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | FB | Feedback input pin. The PWM duty cycle is determined by voltage level into this pin |
| 3 | OTP | Adjustable OTP |
| 4 | CS | Current sense input pin. Connected to MOSFET current sensing resistor node |
| 5 | $V_{CC}$ | Power supply |
| 6 | OUT | The totem-pole output driver for driving the power MOSFET |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 ~ 32 | V |
| Input Voltage to OUT Pin | $V_{OUT}$ | -0.3 ~ $V_{CC}$+0.3 | V |
| FB, CS, OTP | | -0.3 ~ 6 | V |
| Power Dissipation @ $T_A$=+25°C | $P_D$ | 400 | mW |
| Junction Temperature | $T_J$ | +150 | °C |
| Operating Ambient Temperature | $T_{OPR}$ | -40 ~ +125 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 9 ~ 30 | V |
| Start up Resistor | | 0.86 ~ 4.4 | MΩ |
| $V_{CC}$ Capacitor | | 2.2 ~ 4.7 | μF |

## ■ THERMAL DATA

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Junction to Ambient | $\theta_{JA}$ | 250 | °C/W |

## ■ ELECTRICAL CHARACTERISTICS ($V_{CC}$=15V, $T_A$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| $V_{CC}$ (ON) | $V_{CC(ON)}$ | | 15 | 16 | 17 | V |
| $V_{CC}$ (OFF) | $V_{CC(MIN)}$ | | 6.7 | 7.7 | 8.7 | V |
| Startup Current | $I_{STR}$ | $V_{CC}$<$V_{CC(ON)}$-0.5V | | 1 | 5 | μA |
| Operating Current | $I_{OP}$ | $V_{FB}$=3V | | 0.68 | | mA |
| | | $V_{FB}$=Burst Level | | 0.25 | | mA |
| $V_{CC}$ OVP Threshold | $V_{CC(OVP)}$ | | 30 | 32 | 34 | V |
| **OSCILLATOR & SWITCHING FREQUENCY** | | | | | | |
| Switching Frequency | $F_{(SW)}$ | | 60 | 65 | 70 | KHz |
| Temperature Stability | $F_{DT}$ | Guaranteed by Design | | | 10 | % |
| Voltage Stability | $F_{DV}$ | | | | 10 | % |
| Green Mode Frequency | $F_{(SW\_GR)}$ | | 20 | | | KHz |
| Frequency Spreading Range | ΔOSC | | +9 | | -9 | % |
| Max. Duty Cycle | $DC_{MAX}$ | $V_{FB}$=3.9V | 58 | 64 | 71 | % |
| **VOLTAGE FEEDBACK** | | | | | | |
| Open Loop Voltage | $V_{FB\_Open}$ | | 5.00 | 5.40 | 5.80 | V |
| OLP Level | $V_{FB\_OLP}$ | | 4.40 | 4.65 | 4.90 | V |
| OLP De-Bounce Time | $T_{D\_OLP}$ | $V_{FB}$>5V | 44 | 64 | 94 | mS |
| Burst-Mode Enter FB Voltage | $V_{FB-IN}$ | | | 1.05 | | V |
| Burst-Mode Quit FB Voltage | $V_{FB-OUT}$ | | | 1.15 | | V |
| FB Pin Short Current | $I_{FB\_SHORT}$ | | | 60 | | μA |

## ■ ELECTRICAL CHARACTERISTICS (Cont.)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT SENSING** | | | | | | |
| Current Limiting Threshold Voltage with 40% Duty | $V_{CS(OFF)\_40\% Duty}$ | | 0.80 | 0.87 | 0.94 | V |
| Lead Edge Blanking Time | $T_{LEB}$ | Guaranteed by Design | | 350 | | ns |
| SDSP(Secondary Diode Short Protection) CS pin Level | $V_{SCP}$ | Guaranteed by Design | 1.20 | 1.32 | 1.45 | V |
| CS OVP Level | $V_{CS\_OVP}$ | Guaranteed by Design | | 0.2 | | V |
| Soft Start Time | | Guaranteed by Design | | 6 | | mS |
| **GATE DRIVE OUTPUT** | | | | | | |
| Output Low Level | $V_{OL}$ | $V_{CC}$=15V, $I_{OUT}$=-20mA | | | 1 | V |
| Output High Level | $V_{OH}$ | $V_{CC}$=15V, $I_{OUT}$=20mA | 9 | | | V |
| Rising Time | $t_R$ | 10% to 90% of $V_{OUT}$, $C_L$=1nF | | 200 | | nS |
| Falling Time | $t_F$ | 90% to 10% of $V_{OUT}$, $C_L$=1nF | | 60 | | nS |
| Out Clamping | $V_{clamp}$ | $V_{CC}$=20V | | 17 | | V |
| **OTP PIN SECTION** | | | | | | |
| OTP upper source current | $I_{OTP}$ | | 95 | 100 | 105 | μA |
| OTP Threshold Level | $V_{OTP}$ | | 0.90 | 0.95 | 1.00 | V |
| OVP Threshold Level | $V_{OTP\_OVP}$ | Guaranteed by Design | 4.08 | 4.28 | 4.48 | V |
| Protection De-Bounce Time | $T_{DEM\_OTP}$ | Guaranteed by Design | | 7 | | Times |
| **THERMAL SHUT DOWN** | | | | | | |
| Internal OTP Threshold | | | | 150 | | °C |

## ■ APPLICATION NOTE

The UTC **UC3838** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **UC3838** series.

**Start-up Current**

The start-up current is only 1μA. Low start-up current allows a start-up resistor with a high resistance and a low-wattage to supply the start-up power for the controller. For AC/DC adaptor with universal input range design, a 2.5~3MΩ, startup resistor could be used together with a $V_{CC}$ capacitor to provide a fast startup and low power dissipation solution. The D1 IN4148 can improve surge capability to 6.6KV.

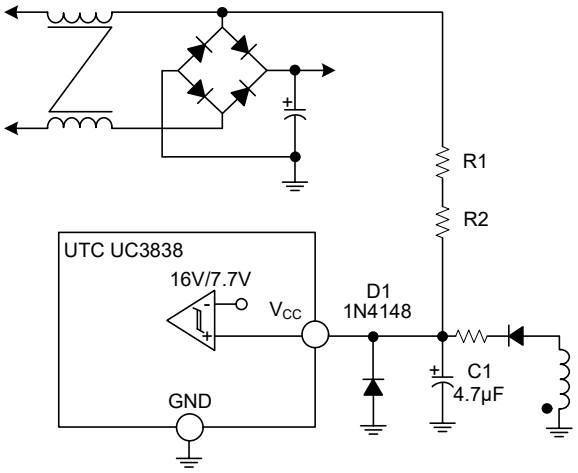



Fig. 1 Startup Circuit

**Operation Mode**

The UTC **UC3838** provides a CCM switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, once if the converter enters into DCM, the UTC **UC3838** automatically finds the local minimum $V_{DS}$ point and switching at this local.

Normally, the conduction loss is dominated at heavy load condition, and the switching loss turns to be larger than conduction loss in light load, especially at 1/4 ~ 1/2 of full load. By this kind of mixed mode operation to have CCM in heavy load and switching in light load can optimize the overall average efficiency during the entire operation range.

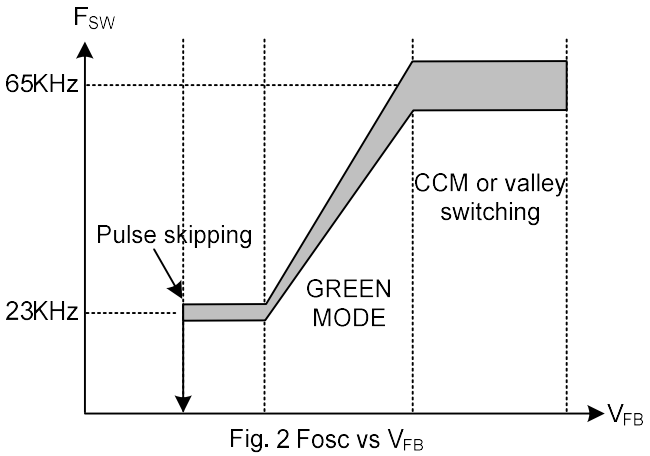



Fig. 2 Fosc vs $V_{FB}$

## ■ APPLICATION NOTE (Cont.)

As shown in Fig. 3, at deep light-load or no-load condition, the switching loss is the dominant factor. To improve the light-load efficiency, burst mode operation will stop the switching cycle of the OUT pin when FB pin voltage is below "$V_{FB\_IN}$" Level and restart the switching cycle of the OUT pin when FB pin voltage is above "$V_{FB\_OUT}$".

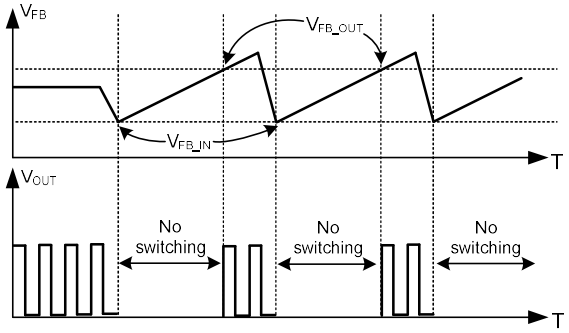



Fig. 3 Burst Mode Operation

**Over Voltage Protection on $V_{CC}$ Pin ( $V_{CC}$ OVP )**

The $V_{CC}$ OVP will shut down the switching of the power MOSFET whenever $V_{CC}$ >$V_{OVP}$. The OVP event as followed Fig.4.

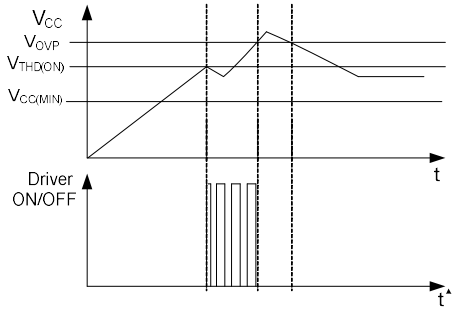



Fig.4 OVP case

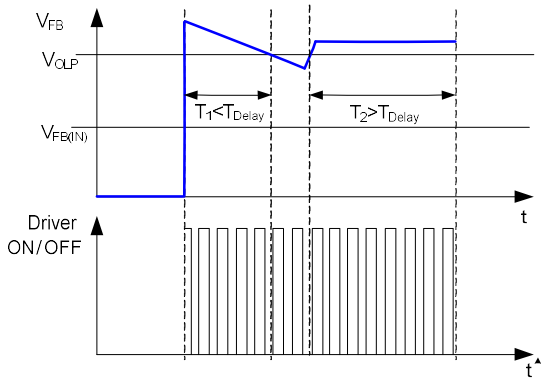



Fig.5 OLP case

**Over Load &Open Loop & Output Short Protection ( OLP or OSP )**

OLP or OSP will shut down driver when $V_{FB}$ > $V_{OLP}$ for continual a blanking time. The OLP or OSP event as followed Fig.5.

**Over Temperature Protection ( OTP )**

OTP will shut down driver when the NTC resistor temperature $T_J$>$T_{(THR)}$. Pull this pin below 0.95V to shutdown the controller into latch mode until AC power-on again

## ■ APPLICATION NOTE (Cont.)

**Adjustable OTP & OVP Protection on OTP PIN**

The OTP circuit is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Once an over-temperature condition is detected, the OTP is enabled to shut down the controller to protect the controller. Typically, a NTC is recommended to connect with OTP pin. The NTC resistance will decrease as the device or ambient in high temperature. The relationship is as below.

$$V_{OTP} = 100\mu A \times R_{NTC}$$

When the $V_{OTP}$ is below the defined voltage threshold (typ. 0.95V), UTC **UC3838** will shutdown the gate output and latch off the power supply. There are 2 conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise $V_{OTP}$ up above 1.05V. Then, VCC recovery, until AC power-on again

An over voltage protection for OTP pin is fulfilled by monitoring the voltage $V_{CC1}$ after the zener connected in series to the VCC. When $V_{CC1}$ exceeds $V_{OTP\_OVP}$ (typ. 4.28V), output will shutdown until AC power-on again.

$$V_{CC(OVP)} = V_{OTP\_OVP+}V_Z$$

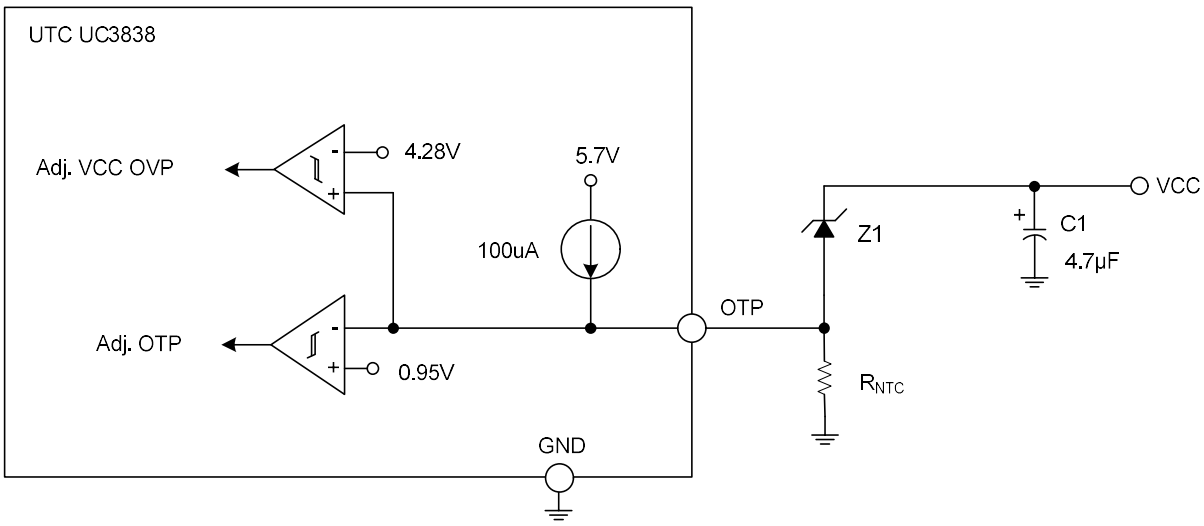



Fig. 6 OTP-Pin Protection

## ■ APPLICATION NOTE (Cont.)

**Cycle by Cycle Over-Current Protection (OCP)**

In a Flyback topology converter, the main MOSFET switch of the Flyback converter turns on and off rapidly. The energy is stored in the inductor when the MOSFET turns on. The inductor current flowing through the sensing resistor ($R_{CS}$) is shown in Fig.7. The current limit is determined by the equation below:

$$I_{PEAK\_MAX} = \frac{V_{CS}}{R_{CS}}$$

In order to prevent the CS pin from false triggering, an internal leading edge blanking time (350nS Typ.) is added and an external low pass RC filter is also recommended to filter the turn-on spike of CS node.

In general, the power converter can deliver more current at high input voltage than at low input voltage. To compensate this, an offset voltage is added to the CS signal by an internal current source ($I_{OCP}$) and an external resistor ($R_{OCP}$) in series between the sense resistor (Rcs) and the CS pin, as shown in Fig.8. By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted. The value of $I_{OCP}$ depends on the duty cycle of OUT pin. The relation curve between $I_{OCP}$ and duty is shown in Figure 7.

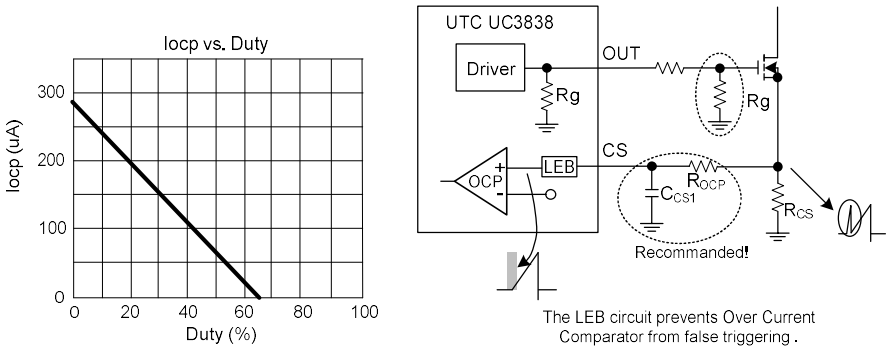



Fig. 7 Current Sensing

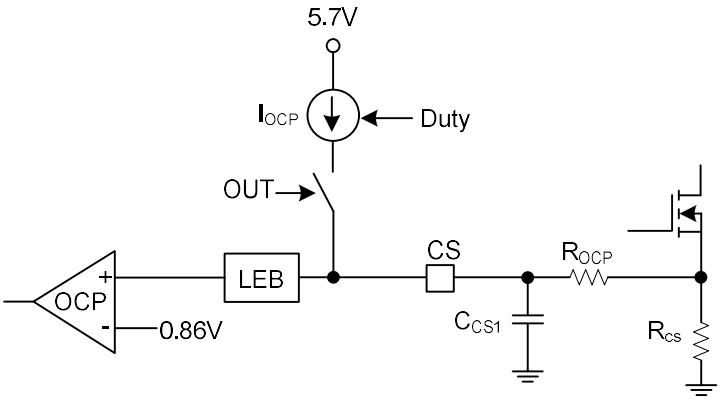
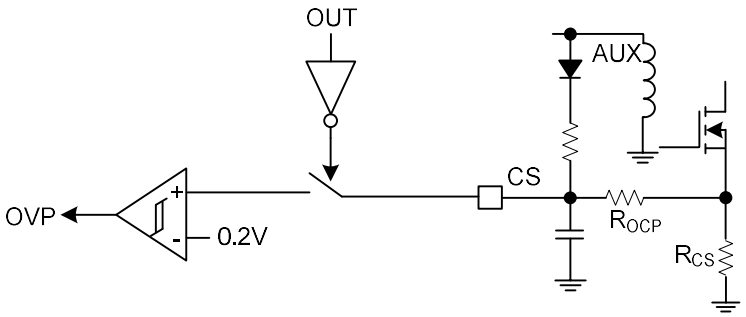



Fig. 8 AC input Compensation ON CS-PIN

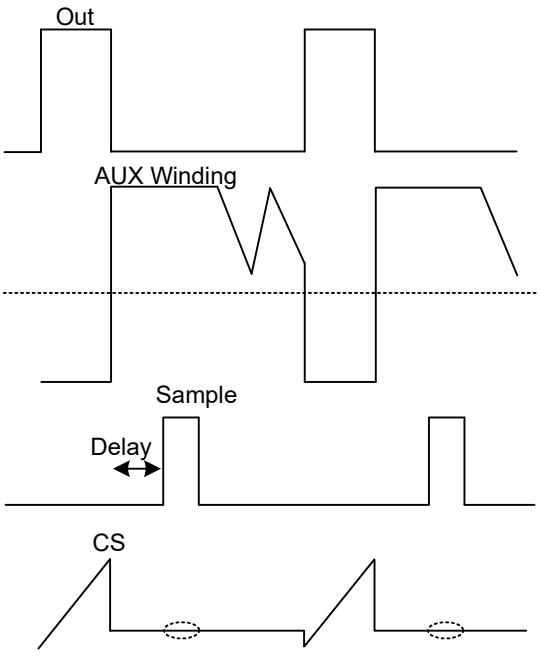
## ■ APPLICATION NOTE (Cont.)

In light load conditions, the offset should be removed since it is in same order of magnitude as the current sense signal. Therefore the compensation current is only fully added when the FB voltage is higher than 2.27V. $R_{OCP}$: 470~1.2k, $C_{OCP}$: 47pF~390pF.

An output overvoltage protection is implemented in the UTC **UC3838**, as shown in Fig. 9. It senses the auxiliary voltage via the divided resistors. The auxiliary winding voltage is reflected from secondary winding and therefore the flat voltage on the CS pin is proportional to the output voltage. UTC **UC3838** can sample this flat voltage level after a delay time to perform output over voltage protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling voltage level is compared with internal threshold voltage 0.2V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, when typically 7 cycles of subsequent OVP events are detected, the OVP circuit switches the power MOSFET off. As the protection is occur, the converter only restarts after VCC auto-recovery.




(a)




(b)

Fig. 9 DCOVP ON CS-PIN

## ■ APPLICATION NOTE (Cont.)

**MOSFET Characteristic**

The MOSFET is divided into three operation regions, ohmic region, saturation region, and the cut-off region, shown as Fig. 10(a). For switching power supply applications, it shall operate in ohmic and cut-off region. Never reach the region of saturation; it would cause damage for acting beyond the maximum safety operating area. It's necessary to check the characteristic of MOSFET. Fig.10(c) shows a totem pole architecture for the circuit of OUT. The output high level of OUT is at around $V_{CC}$-1.5V. Refer to on-region characteristics of the MOSFET, check the saturation current of $V_{GS}H(MIN)$ to make sure the saturation current is high enough to activate MOSFET to operate in ohmic region. In order not to decrease the voltage across $V_G$, it's recommended not to connect a forward diode between the gate of the MOSFET and OUT pin, for example like Fig.10(d) . In addition, pulling $V_{CC}$ level high can keep $V_{GSH}$ in high level, for example:

(1). Increase NX value to pull $V_{CC}$ level high. (2). Increase $V_{CC}$ capacitance to improve $V_{CC}$'s performance to drop at startup transient, shown as Fig.10(b) .

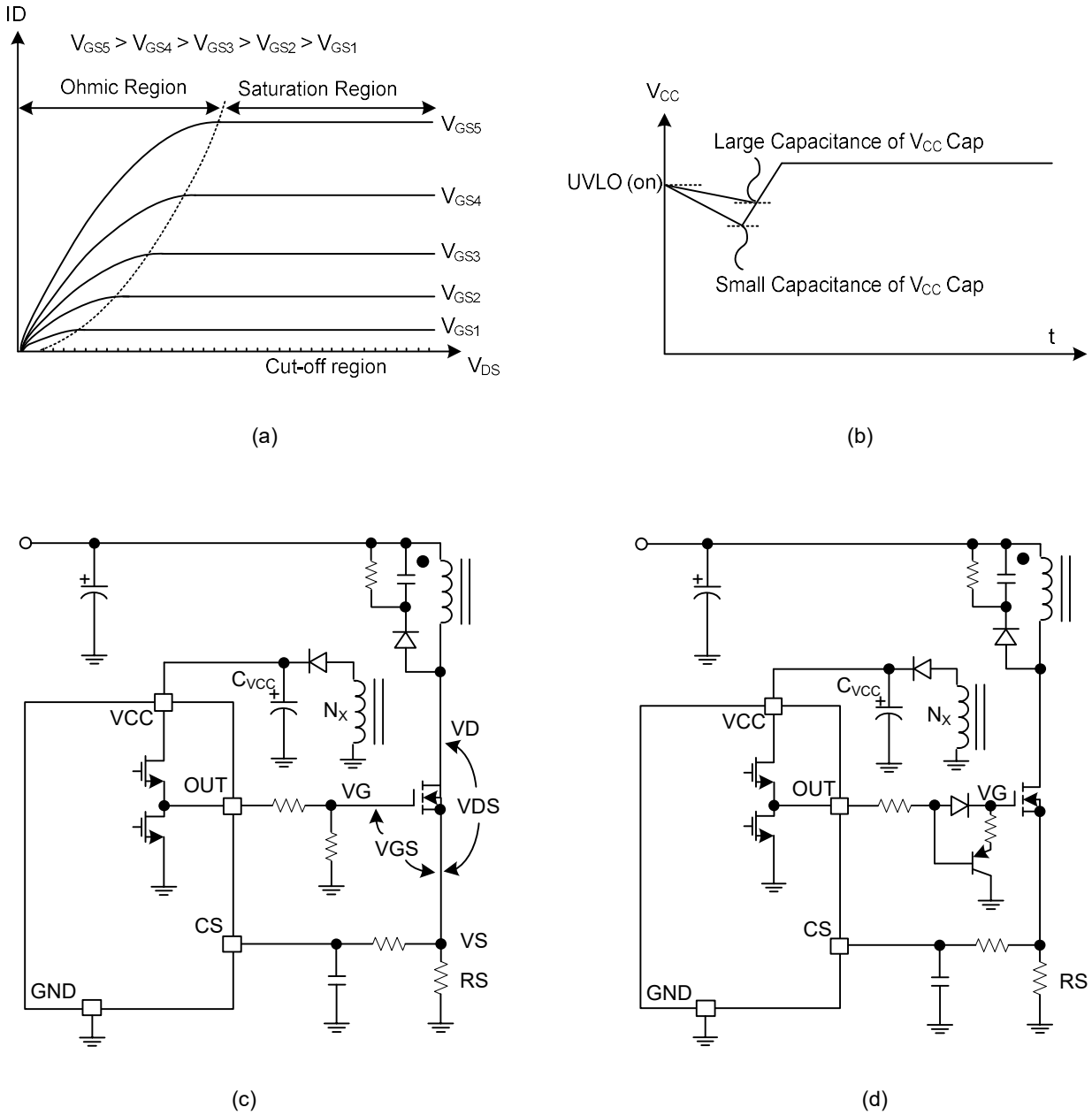



Fig.10 MOSFET Characteristic

## ■ TYPICAL APPLICATION CIRCUIT