



UT30NN06

POWER MOSFET

30A, 60V N-CHANNEL POWER MOSFET

DESCRIPTION

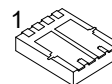
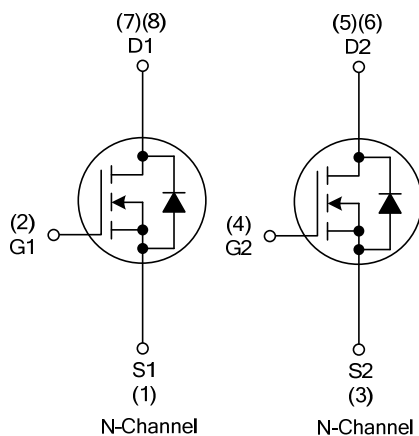
The UTC **UT30NN06** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance, low gate charge and high switching speed.

The UTC **UT30NN06** is suitable for high voltage synchronous rectifier and DC/DC converters, etc.

FEATURES

- * $R_{DS(ON)} \leq 32 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=15\text{A}$
 $R_{DS(ON)} \leq 40 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=15\text{A}$
- * High Switching Speed
- * High Cell Density Trench Technology

SYMBOL



PDFN5×6

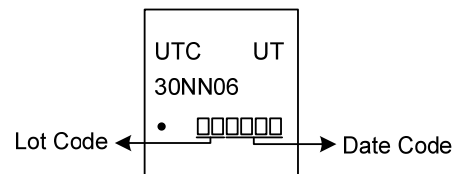
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT30NN06L-P5060-R	UT30NN06G-P5060-R	PDFN5×6	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT30NN06G-P5060-R 		(1) R: Tape Reel (2) P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	15	A
	Pulsed (Note 2)	I_{DM}	30	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	25	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.1	V/nS
Power Dissipation (Note 5)		P_D	20	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L=0.1\text{mH}$, $I_{AS}=22\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	35	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	6.25	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

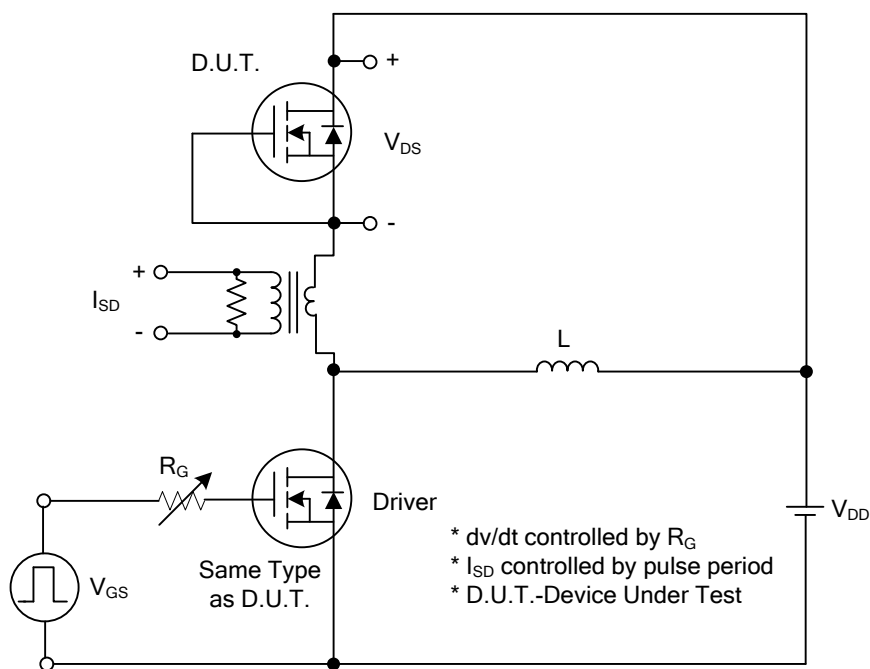
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =15A		26	32	mΩ
			V _{GS} =4.5V, I _D =15A		30	40	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		1780		pF
Output Capacitance		C _{OSS}			98		pF
Reverse Transfer Capacitance		C _{RSS}			72		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =48V, V _{GS} =10V, I _D =30A (Note 1, 2)		40		nC
Gate to Source Charge		Q _{GS}			11		nC
Gate to Drain Charge		Q _{GD}			6		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =30V, V _{GS} =10V, I _D =30A, R _G =3Ω (Note 1, 2)		17		ns
Rise Time		t _R			16.5		ns
Turn-off Delay Time		t _{D(OFF)}			44		ns
Fall-Time		t _F			17		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				15	A
Maximum Body-Diode Pulsed Current		I _{SM}				30	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =30A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)		t _{rr}	I _S =30A, V _{GS} =0V,		52		nS
Reverse Recovery Charge		Q _{rr}	dl/dt=100A/μs		30		nC

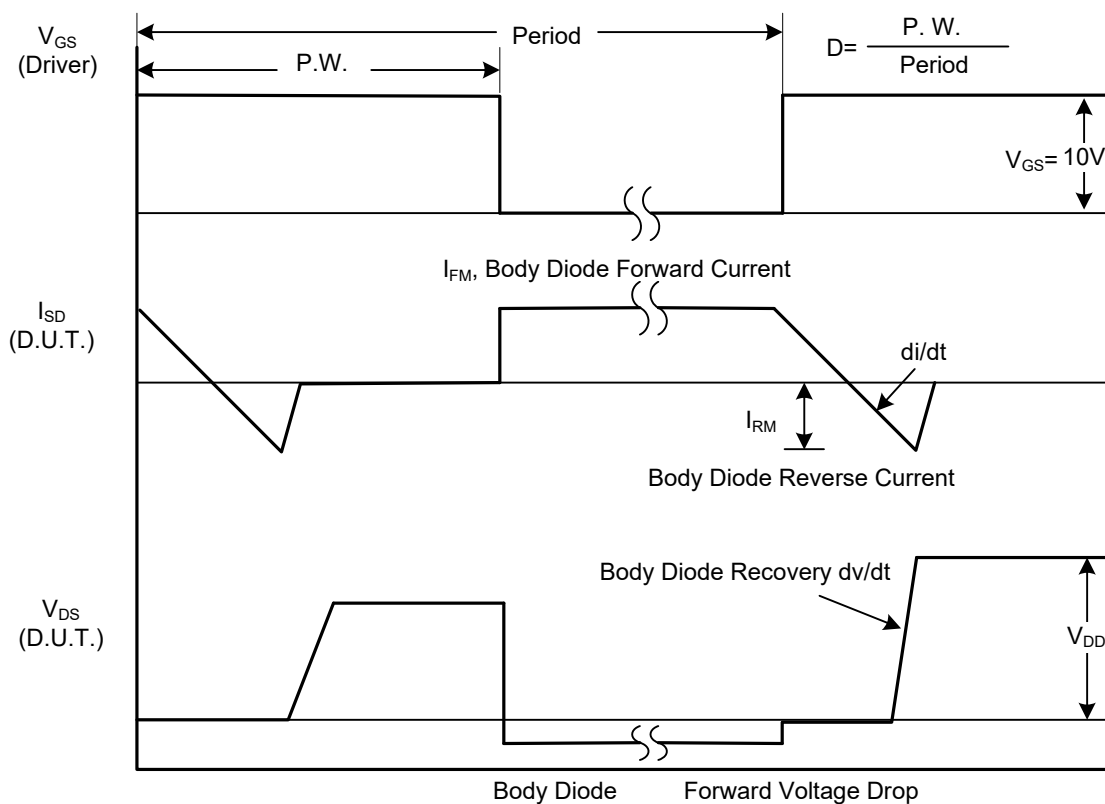
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

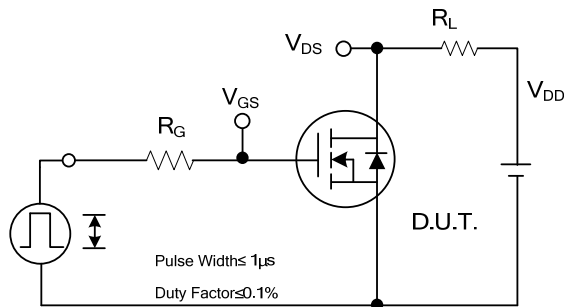


Peak Diode Recovery dv/dt Test Circuit

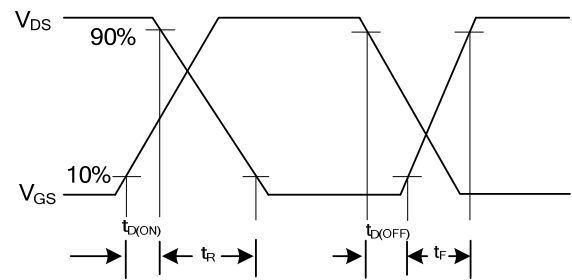


Peak Diode Recovery dv/dt Waveforms

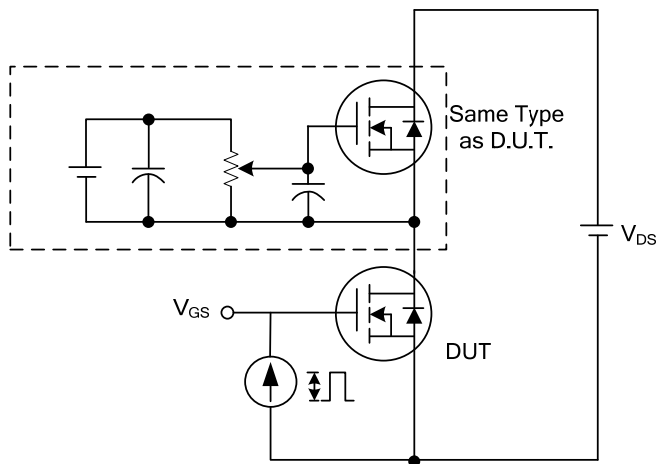
■ TEST CIRCUITS AND WAVEFORMS



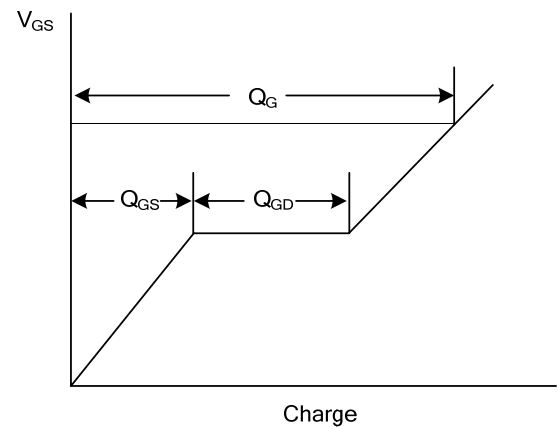
Switching Test Circuit



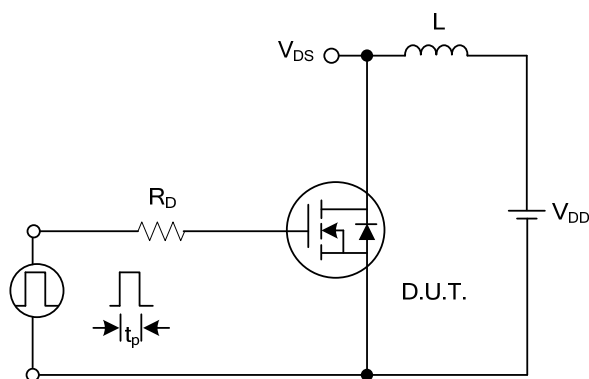
Switching Waveforms



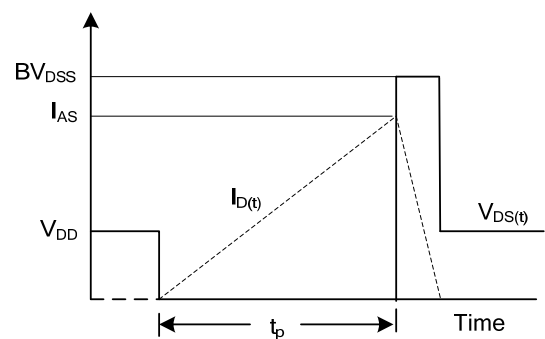
Gate Charge Test Circuit



Gate Charge Waveform

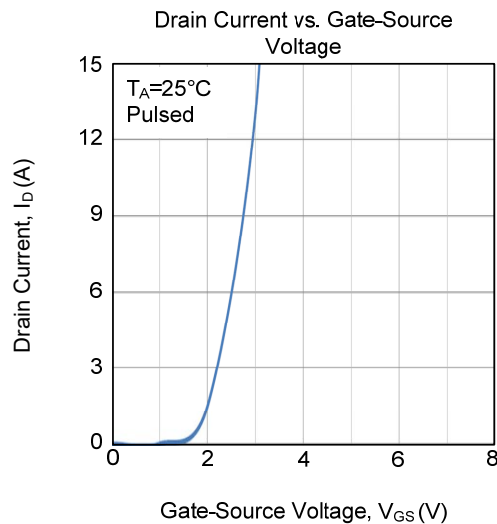
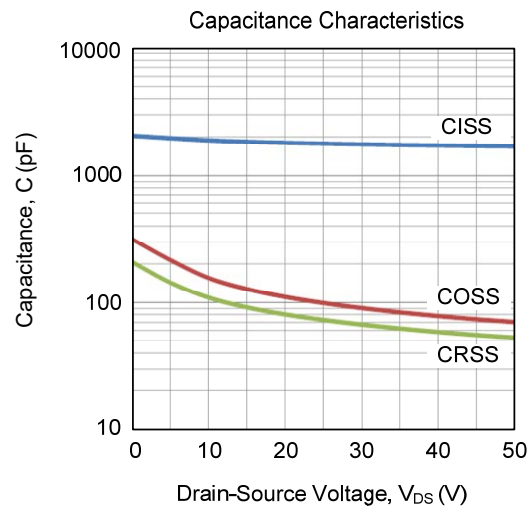
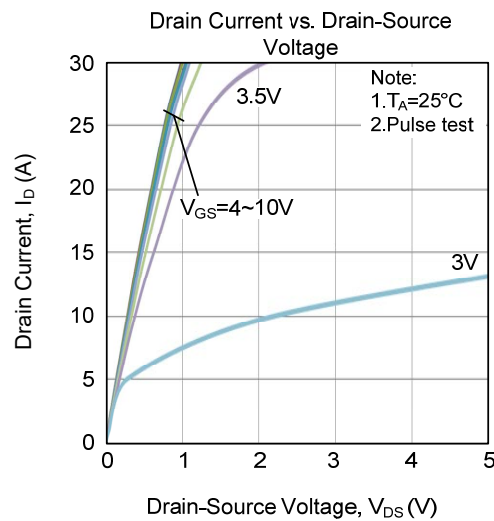


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

TYPICAL CHARACTERISTICS



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