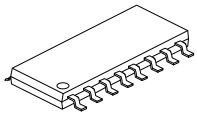
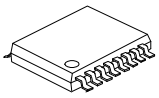
U74AHC595B

CMOS IC

8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS



SOP-16



TSSOP-16

■ DESCRIPTION

The UTC **U74AHC595B** contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs, except $Q_{H'}$, are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together the shift register always is one clock pulse ahead of the storage register.

■ FEATURES

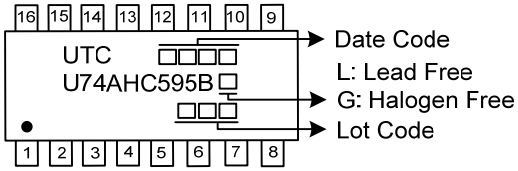
* Operation Voltage Range: 2 ~ 5.5V
* Shift Register Has Direct Clear
* 8-bit Serial-In, Parallel-Out Shift

■ ORDERING INFORMATION

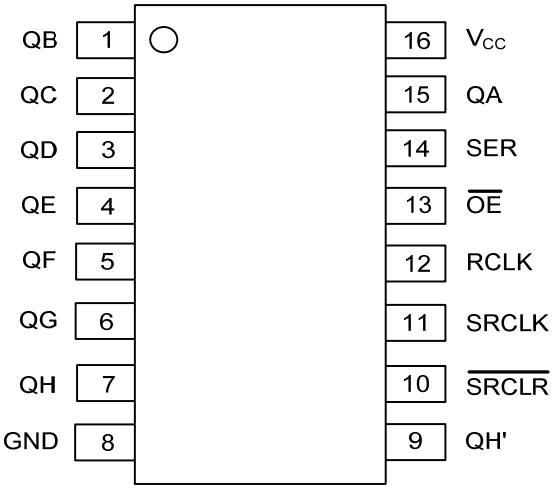
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC595BL-S16-R	U74AHC595BG-S16-R	SOP-16	Tape Reel
U74AHC595BL-P16-R	U74AHC595BG-P16-R	TSSOP-16	Tape Reel

U74AHC595BG-S16-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) S16: SOP-16, P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

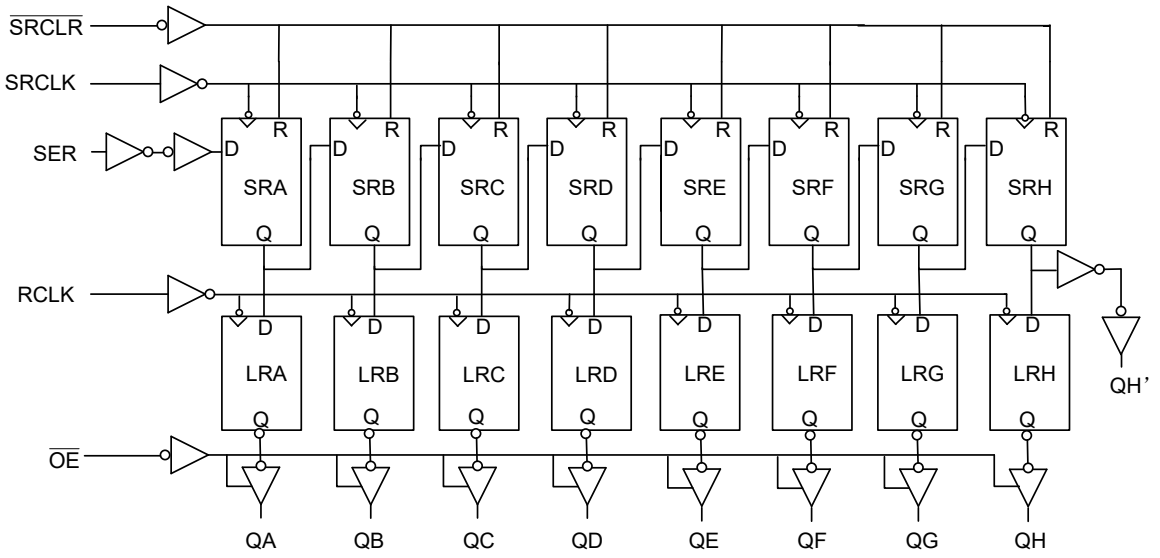


■ FUNCTION TABLE

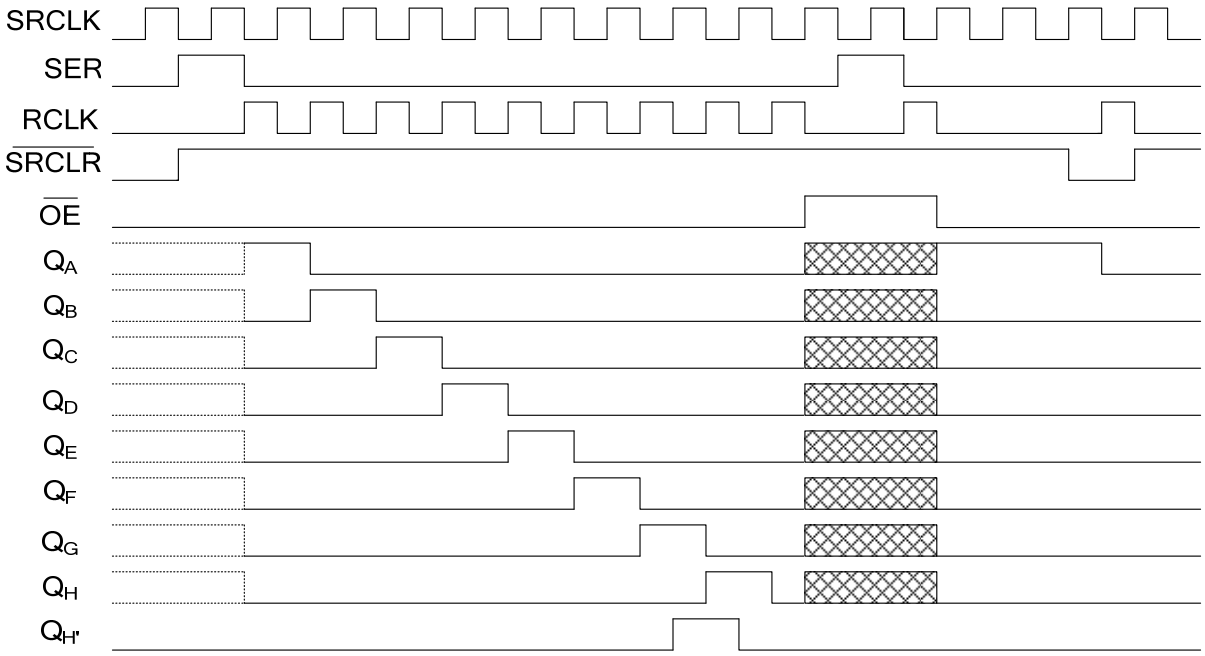
FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note:H : HIGH voltage level.
L : LOW voltage level.
X : Don't care.
Z : High impedance OFF-state.
NC: No change.
↑ : Low-to-High transition.
↓ : High-to-Low transition.

■ LOGIC DIAGRAM (POSITIVE LOGIC)



■ TIMING DIAGRAM



Note: ▨ Implies that the outputs is in 3-State mode.

■ ABSOLUTE MAXIMUM RATING (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ 7.0	V
Output Voltage (Active Mode)	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Clamp Current (V_{IN} <0)	I_{IK}	-20	mA
Output Clamp Current (V_{OUT} <0 or V_{OUT} >V_{CC})	I_{OK} (Note 2)	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±75	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	θ_{JA}	73	°C/W
	TSSOP-16		108	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2		5.5	V
Input Voltage		V_{IN}	0		5.5	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Input Transition Rise or Fall Rate	V_{CC}=3.3±0.3V	Δt/Δv			100	ns/V
	V_{CC}=5±0.5V				20	ns/V
Operating Temperature		T_A	-40		+125	°C

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V_{IH}	V_{CC}=2V	1.5			1.5			V
		V_{CC}=3V	2.1			2.1			
		V_{CC}=5.5V	3.85			3.85			
Low-Level Input Voltage	V_{IL}	V_{CC}=2V			0.5			0.5	V
		V_{CC}=3V			0.9			0.9	
		V_{CC}=5.5V			1.65			1.65	
High-Level Output Voltage	V_{OH}	V_{CC}=2V, I_{OH}=-50μA	1.9	2		1.9			V
		V_{CC}=3V, I_{OH}=-50μA	2.9	3		2.9			
		V_{CC}=4.5V, I_{OH}=-50μA	4.4	4.5		4.4			
		V_{CC}=3V, I_{OH}=-4mA	2.58			2.40			
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			3.70			
Low-Level Output Voltage	V_{OL}	V_{CC}=2V, I_{OL}=50μA			0.1			0.1	V
		V_{CC}=3V, I_{OL}=50μA			0.1			0.1	
		V_{CC}=4.5V, I_{OL}=50μA			0.1			0.1	
		V_{CC}=3V, I_{OL}=4mA			0.36			0.55	
		V_{CC}=4.5V, I_{OL}=8mA			0.36			0.55	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0 ~ 5.5V, I_{IN}=5.5V or GND			±0.1			±2	μA
Output Off-State Current	I_{OZ}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, V_{OUT}=V_{CC} or GND, $\overline{OE}$ =V_{IH} or V_{IL}			±0.25			±10	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=GND or V_{CC}, I_{OUT}=0			4			80	μA

■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Clock Frequency	f_{max}	V_{CC}=3.3±0.3V	C_L=15pF	8	13		5			MHz
			C_L=50pF	7.5	12		4			MHz
		V_{CC}=5±0.5V	C_L=15pF	18	33		12			MHz
			C_L=50pF	16	28		10			MHz
Propagation Delay From Input RCLK to Output Q_A-Q_H	t_{PLH}	V_{CC}=3.3±0.3V	C_L=15pF		10	14			16	ns
			C_L=50pF		12	17			19	ns
		V_{CC}=5±0.5V	C_L=15pF		7	10			12	ns
			C_L=50pF		8	12			14	ns
	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		11	14			16	ns
			C_L=50pF		12	17			19	ns
		V_{CC}=5±0.5V	C_L=15pF		7	10			12	ns
			C_L=50pF		9	12			14	ns
Propagation Delay From Input SRCLK to Output QH'	t_{PLH}	V_{CC}=3.3±0.3V	C_L=15pF		75	115			200	ns
			C_L=50pF		80	120			210	ns
		V_{CC}=5±0.5V	C_L=15pF		30	50			90	ns
			C_L=50pF		35	60			100	ns
	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		75	115			200	ns
			C_L=50pF		80	120			210	ns
		V_{CC}=5±0.5V	C_L=15pF		30	50			90	ns
			C_L=50pF		35	60			100	ns
Propagation Delay From Input $\overline{SRCLR}$ to Output QH'	t_{PHL}	V_{CC}=3.3±0.3V	C_L=15pF		80	120			220	ns
			C_L=50pF		83	125			230	ns
		V_{CC}=5±0.5V	C_L=15pF		26	45			80	ns
			C_L=50pF		30	50			90	ns
Propagation Delay From Input $\overline{OE}$ to Output Q_A-Q_H	t_{PZH}	V_{CC}=3.3±0.3V	C_L=15pF		10	12			15	ns
			C_L=50pF		11	15			18.5	ns
		V_{CC}=5±0.5V	C_L=15pF		6	8.6			11	ns
			C_L=50pF		7	10.6			13	ns
	t_{PZL}	V_{CC}=3.3±0.3V	C_L=15pF		9	11.5			15.0	ns
			C_L=50pF		10	15			18.5	ns
		V_{CC}=5±0.5V	C_L=15pF		6	8.6			11	ns
			C_L=50pF		7	10.6			13	ns
Propagation Delay From Input $\overline{OE}$ to Output Q_A-Q_H	t_{PHZ}	V_{CC}=3.3±0.3V	C_L=50pF		11	15.7			17.5	ns
		V_{CC}=5±0.5V			8	10.3			12	ns
	t_{PLZ}	V_{CC}=3.3±0.3V			9	15.7			17.5	ns
		V_{CC}=5±0.5V			7	10.3			12	ns

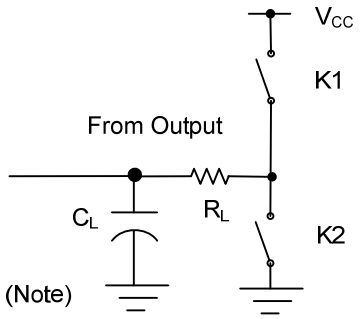
■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Pulse Duration, SRCLK High or Low	t_W	V_{CC}=3.3±0.3V	5			5			ns
		V_{CC}=5±0.5V	5			5			ns
Pulse Duration, RCLK High or Low		V_{CC}=3.3±0.3V	5			5			ns
		V_{CC}=5±0.5V	5			5			ns
Pulse Duration, $\overline{\text{SRCLR}}$ Low		V_{CC}=3.3±0.3V	5			5			ns
		V_{CC}=5±0.5V	5			5			ns
Setup Time, SER Before SRCLK↑	t_{SU}	V_{CC}=3.3±0.3V	3.5			3.5			ns
		V_{CC}=5±0.5V	3			3			ns
Setup Time, SRCLK↑ Before RCLK↑		V_{CC}=3.3±0.3V	8			8			ns
		V_{CC}=5±0.5V	5			5			ns
Setup Time, $\overline{\text{SRCLR}}$ Low Before RCLK↑		V_{CC}=3.3±0.3V	8			8			ns
		V_{CC}=5±0.5V	5			5			ns
Setup Time, $\overline{\text{SRCLR}}$ high (Inactive) Before SRCLK↑		V_{CC}=3.3±0.3V	3			3			ns
		V_{CC}=5±0.5V	2.5			2.5			ns
Hold Time, SER After SRCLK↑	t_H	V_{CC}=3.3±0.3V	1.5			1.5			ns
		V_{CC}=5±0.5V	2			2			ns

■ OPERATING CHARACTERISTICS (V_{CC}=5V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{CC}=5V, V_{IN}=V_{CC} or GND		3	10	pF
Output Capacitance	C_{OUT}	V_{CC}=5V, V_{OUT}=V_{CC} or GND		5.5		pF
Power Dissipation Capacitance	C_{PD}	No load, f=1MHz		25.2		pF

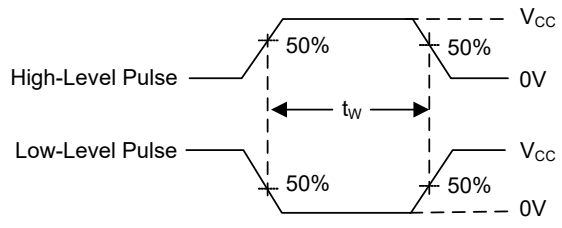
■ TEST CIRCUIT AND WAVEFORMS



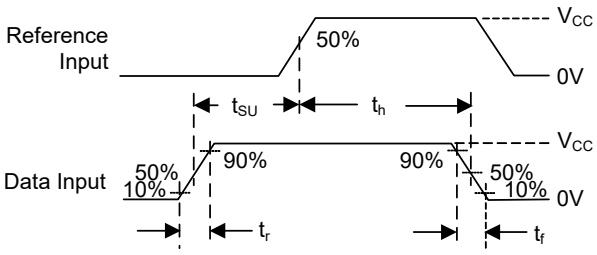
TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

t_{PD} is the same as t_{PHL} and t_{PLH}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

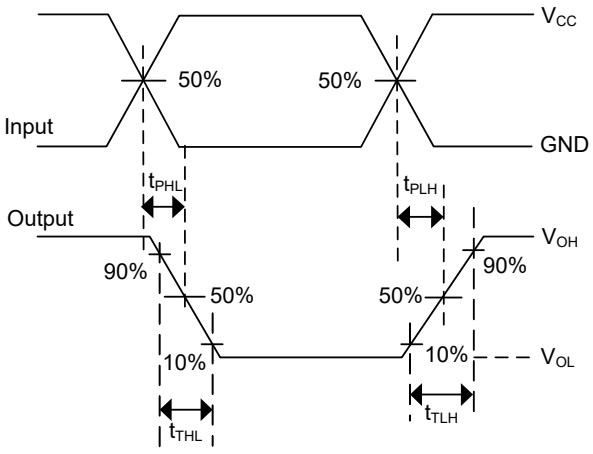
Note: C_L includes probe and jig capacitance. C_L=15pF or 50pF, R_L=1KΩ



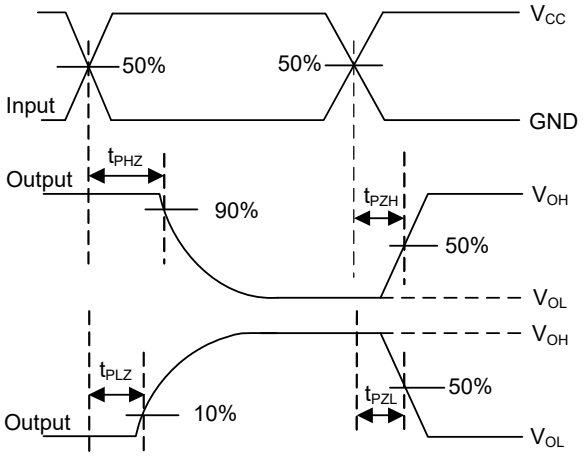
Voltage Waveforms, Pulse Duration



Voltage Waveforms



Voltage Waveforms Propagation Delays



Voltage Waveforms Propagation Delays

Note: All input pulses are supplied by generators having the following characteristics:
P_{RR} ≤ 1MHZ, Z_O = 50Ω, t_r ≤ 3ns, t_f ≤ 3ns.