

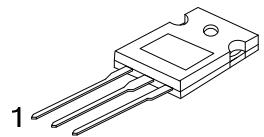
15NK90Z

POWER MOSFET

15A, 900V N-CHANNEL POWER MOSFET

■ DESCRIPTION

The UTC **15NK90Z** is a silicon N-channel MOSFET, it uses UTC's advanced technology to provide the customers with a minimum on state resistance, high switching speed and low gate charge.

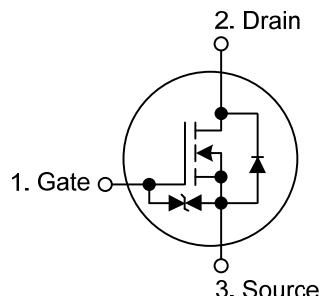


TO-247

■ FEATURES

- * $R_{DS(ON)} \leq 0.40 \Omega$ @ $V_{GS}=10V$, $I_D=7.5A$
- * High switching speed
- * Low input capacitance
- * With ESD protection

■ SYMBOL



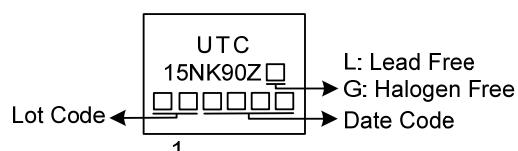
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
15NK90ZL-T47-T	15NK90ZG-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

15NK90ZG-T47-T 	(1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) T47: TO-247 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ ABSOLUTE MAXIMUM RATING ($T_c=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	900	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	DC	I_D	15	A
	Pulsed (Note 2)	I_{DM}	45	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	2888	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.4	V/ns
Power Dissipation		P_D	500	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L = 100mH, $I_{AS} = 7.6\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 15\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	50	$^\circ\text{C/W}$
Junction to Case	θ_{JC}	0.25	$^\circ\text{C/W}$

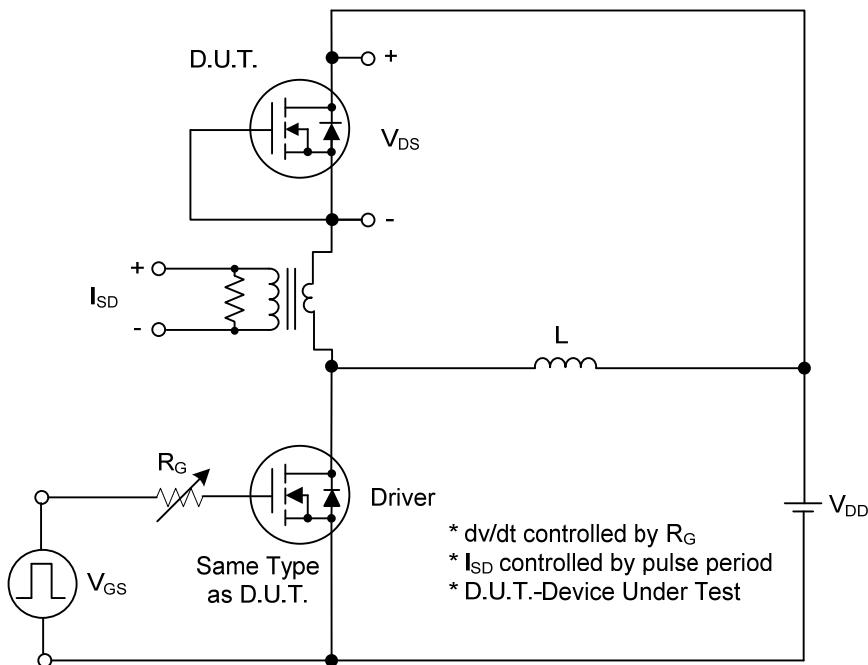
■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	900			V
Drain-Source Leakage Current	I_{DSS}	$V_{\text{DS}}=900\text{V}, V_{\text{GS}}=0\text{V}$			10	μA
Gate-Source Leakage Current	Forward	$V_{\text{GS}}=+20\text{V}, V_{\text{DS}}=0\text{V}$			+10	μA
	Reverse	$V_{\text{GS}}=-20\text{V}, V_{\text{DS}}=0\text{V}$			-10	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{\text{GS(TH)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	3.0		5.0	V
Static Drain-Source On-State Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=7.5\text{A}$		0.32	0.40	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=25\text{V}, f=1.0\text{MHz}$		7000		pF
Output Capacitance	C_{OSS}			510		pF
Reverse Transfer Capacitance	C_{RSS}			40		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{\text{DS}}=720\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=15\text{A}$ (Note 1, 2)		152		nC
Gate to Source Charge	Q_{GS}			45		nC
Gate to Drain Charge	Q_{GD}			40		nC
Turn-ON Delay Time	$t_{\text{D(ON)}}$	$V_{\text{DD}}=100\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=15\text{A}, R_G=25\Omega$ (Note 1, 2)		102		ns
Rise Time	t_R			45		ns
Turn-OFF Delay Time	$t_{\text{D(OFF)}}$			383		ns
Fall-Time	t_F			108		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				15	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				45	A
Diode Forward Voltage	V_{SD}	$I_F=15\text{A}, V_{\text{GS}}=0\text{V}$			1.4	V
Reverse Recovery Time	t_{rr}	$I_S=15\text{A}, V_{\text{GS}}=0\text{V}, \frac{dI_F}{dt} = 100 \text{ A}/\mu\text{s}$		1000		ns
Reverse Recovery Charge (Note 1)	Q_{rr}				16.5	μC

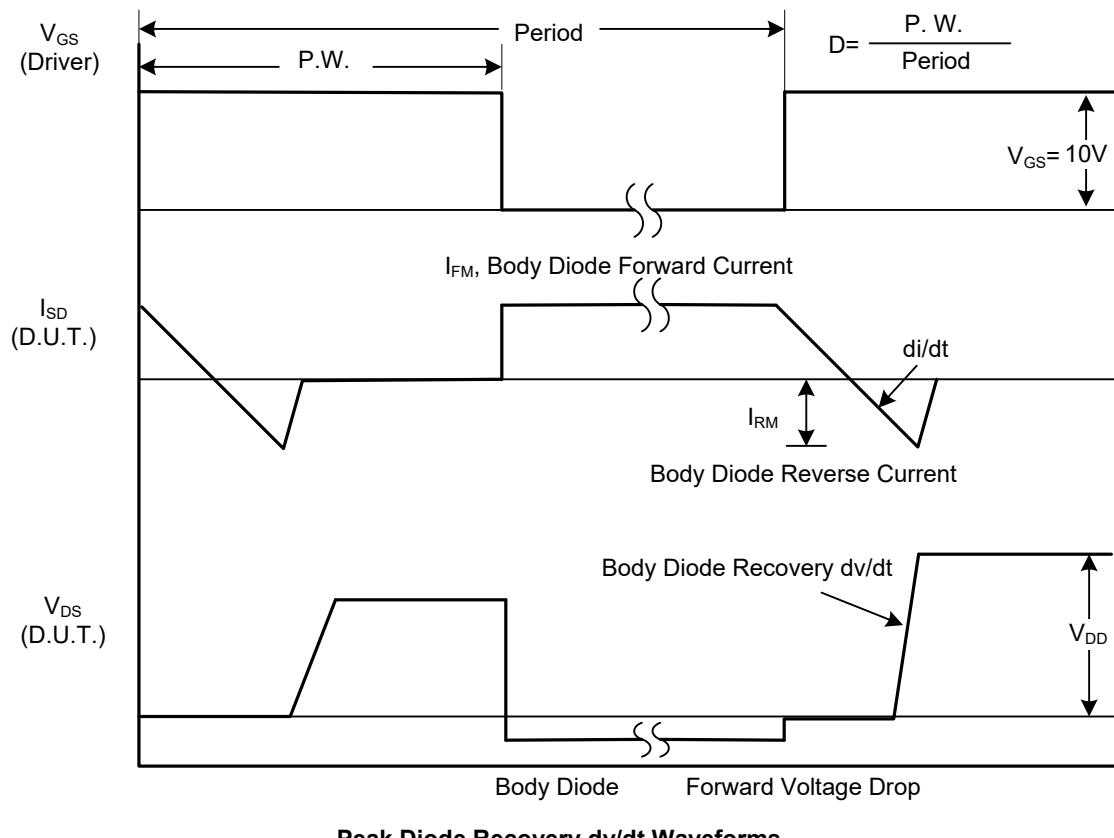
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

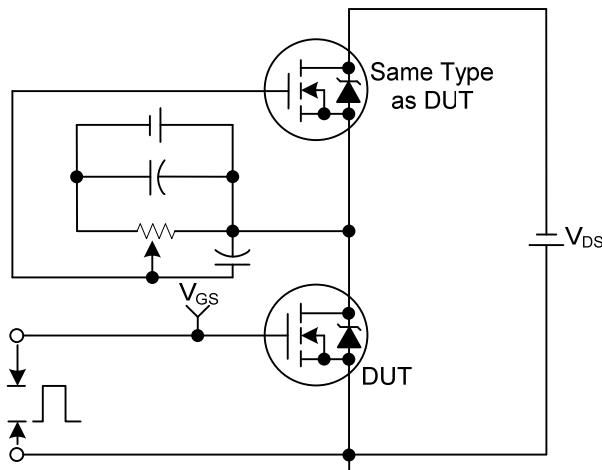


Peak Diode Recovery dv/dt Test Circuit

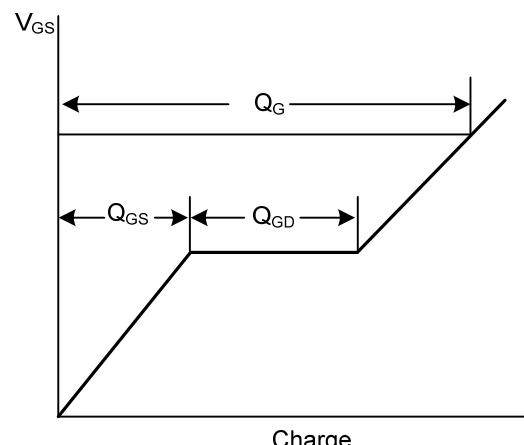


Peak Diode Recovery dv/dt Waveforms

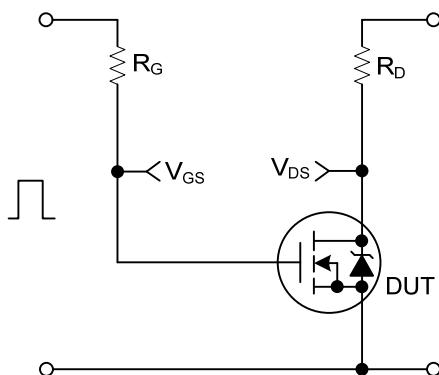
■ TEST CIRCUITS AND WAVEFORMS



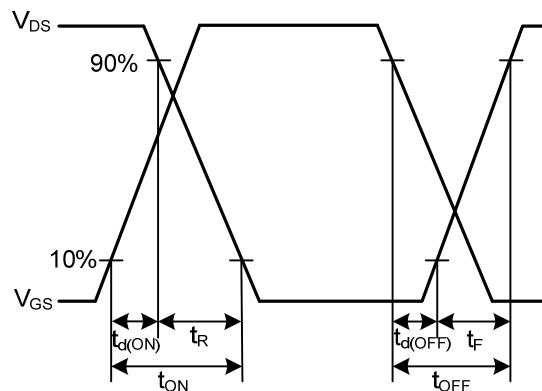
Gate Charge Test Circuit



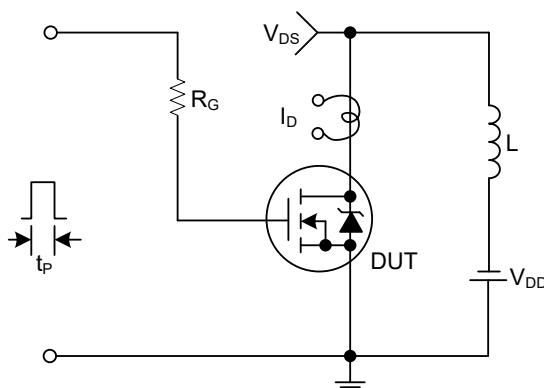
Gate Charge Waveforms



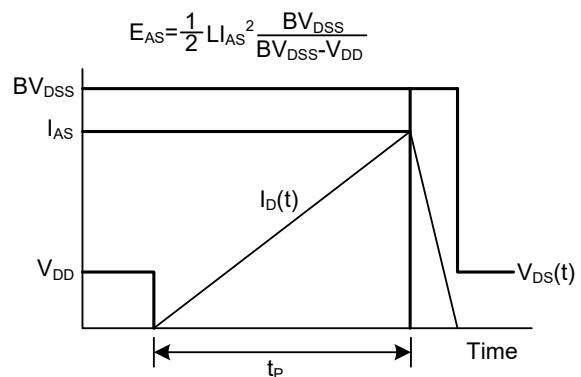
Resistive Switching Test Circuit



Resistive Switching Waveforms

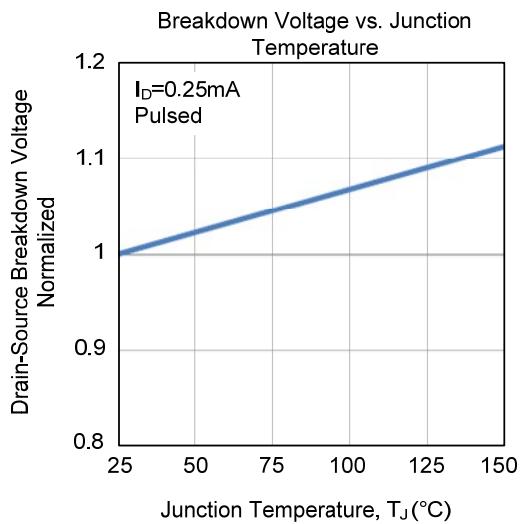
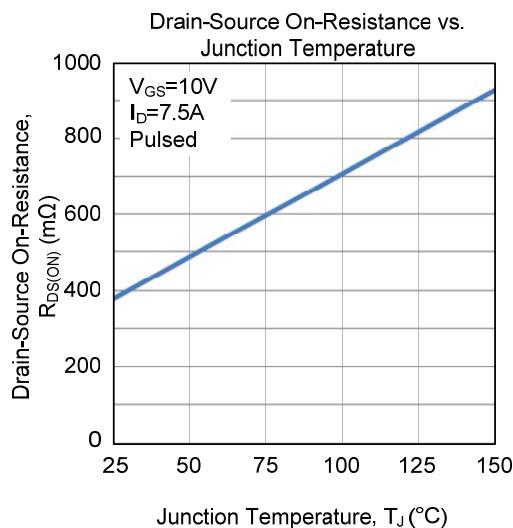
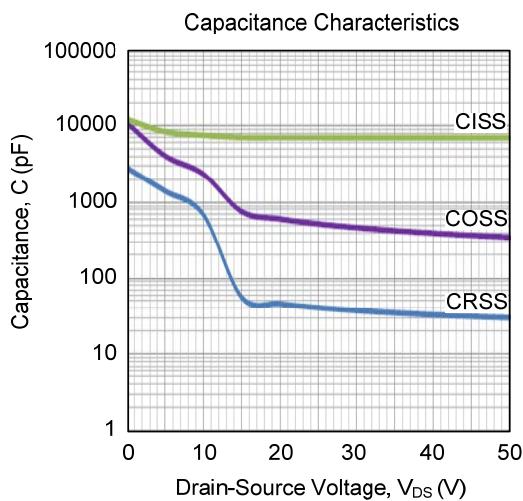
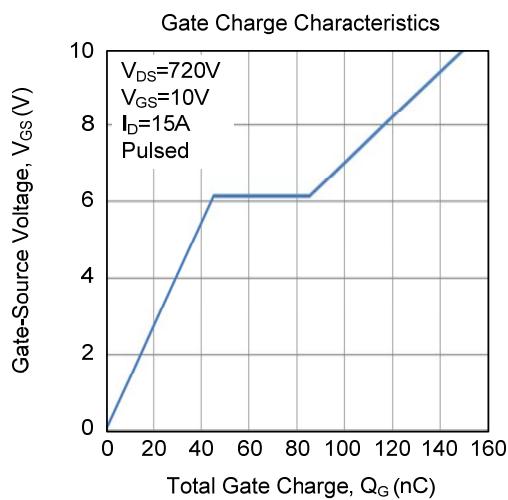
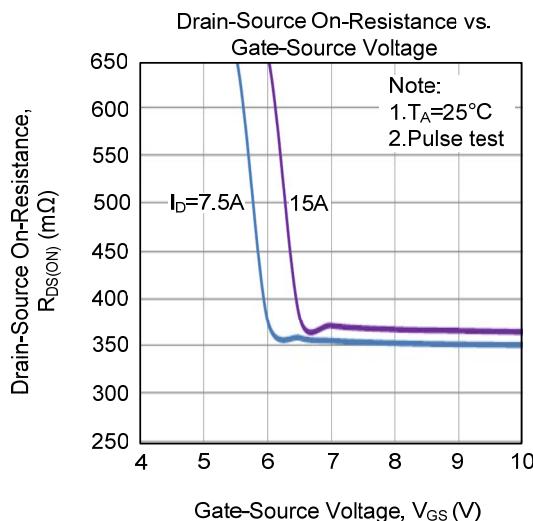
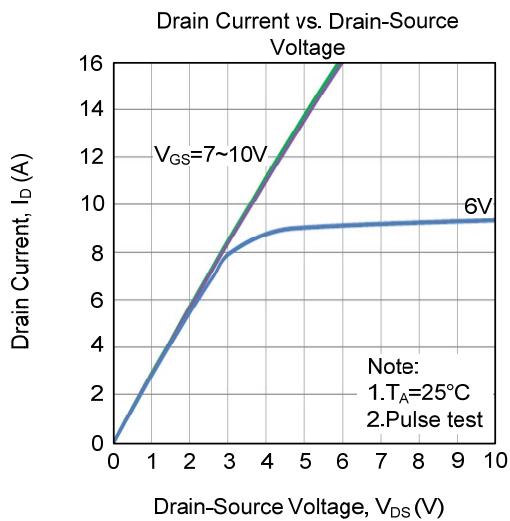


Unclamped Inductive Switching Test Circuit

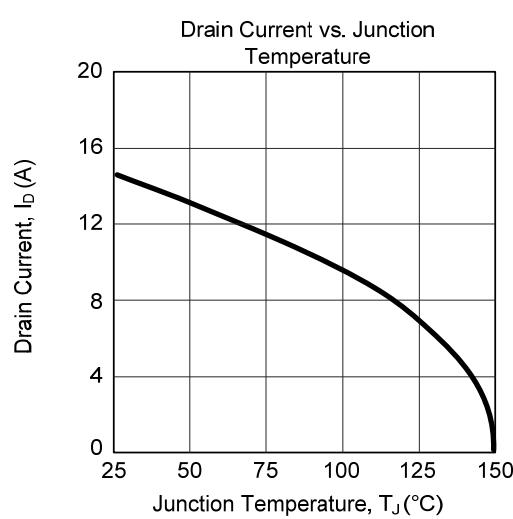
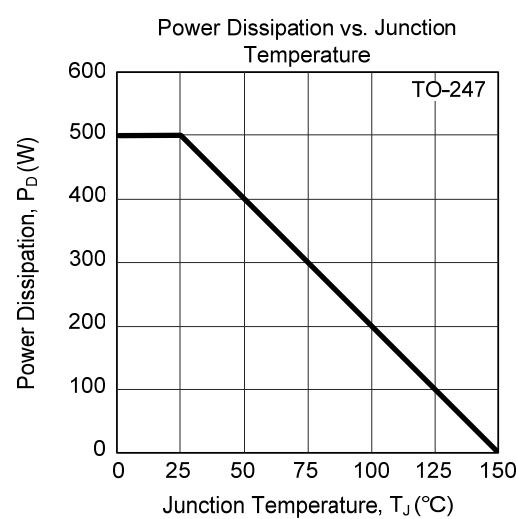
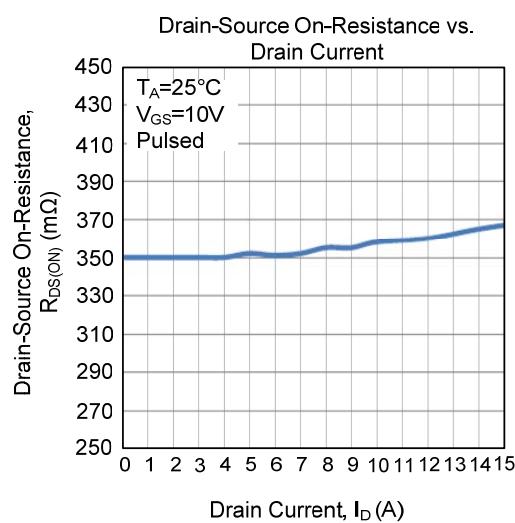
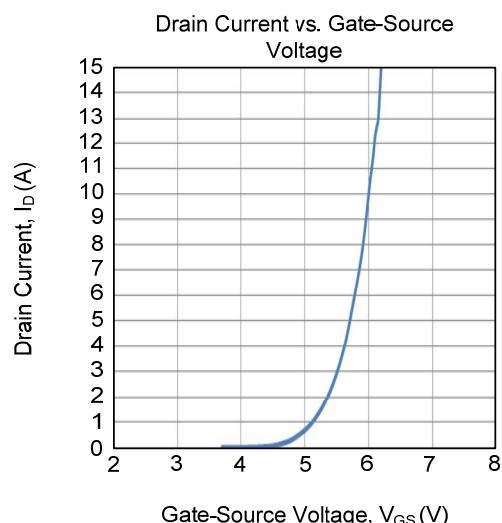
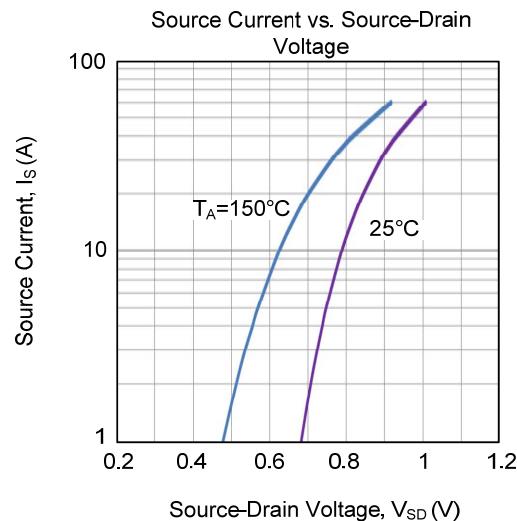
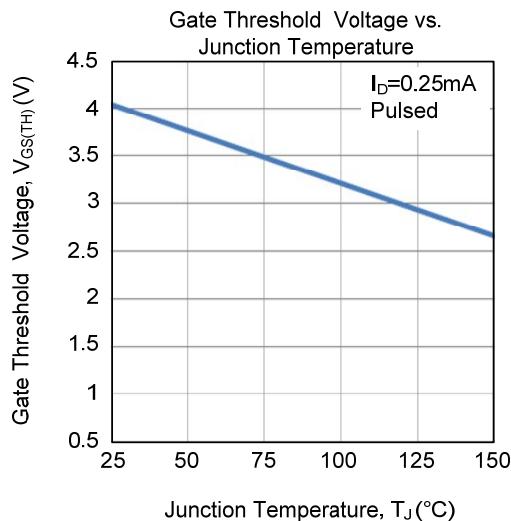


Unclamped Inductive Switching Waveforms

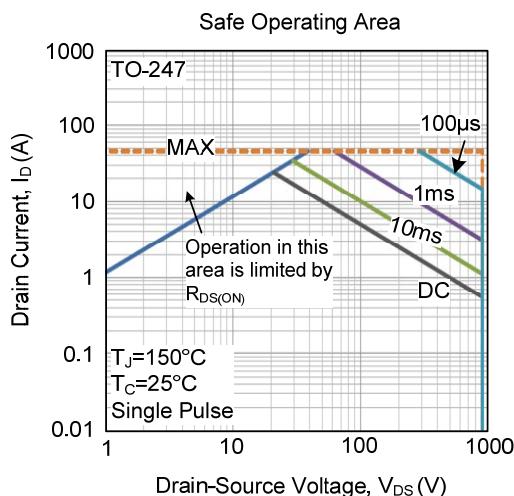
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



- TYPICAL CHARACTERISTICS (Cont.)



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