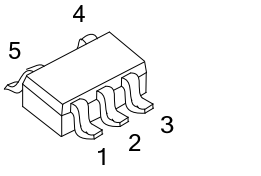
3V LVDS SINGLE HIGH SPEED DIFFERENTIAL DRIVER



SOT-25

■ DESCRIPTION

The UTC **UDS90LV011** is a single LVDS driver device optimized for high data rate and low power applications. The **UDS90LV011** is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is designed to support data rates in excess of 400Mbps (200MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The device is LVDS outputs have been arranged for easy PCB Layout. The differential driver outputs provide low EMI with its typical low output swing of 350 mV. The **UDS90LV011** can be paired with its companion single line receiver, with any of UTC's LVDS receivers, to provide a high-speed LVDS interface.

■ FEATURES

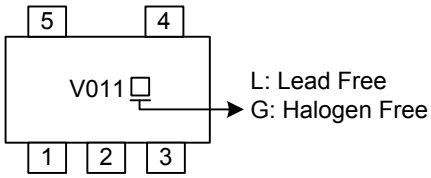
* >400Mbps (200MHz) Switching Rates
* 700 ps (100 ps Typical) Maximum Differential Skew
* 1.5 ns Maximum Propagation Delay
* Single 3.3V Power Supply
* ±400 mV Differential Signaling
* Power Off Protection (Outputs in TRI-STATE)
* Pinout Simplifies PCB Layout
* Low Power Dissipation (23 mW @ 3.3V Typical)
* Fabricated with Advanced CMOS Process Technology

■ ORDERING INFORMATION

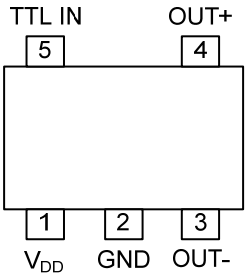
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UDS90LV011L-AF5-R	UDS90LV011G-AF5-R	SOT-25	Tape Reel

UDS90LV011G-AF5-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AF5: SOT-25 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



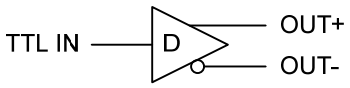
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{DD}	Power supply pin, +3.3V ± 0.3V
2	GND	Ground pin
3	OUT-	Inverting driver output pin
4	OUT+	Non-inverting driver output pin
5	TTL IN	LVTTL/LVCMOS driver input pins

■ FUNCTIONAL DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +4.0	V
LVCMOS input voltage	TTL IN	-0.3 ~ +3.6	V
LVDS output voltage	OUT±	-0.3 ~ +3.9	V
LVDS output short circuit current		24	mA
Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{STG}	-65~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Operating Temperature	T_A	-40		+85	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	277	°C/W

■ ELECTRICAL CHARACTERISTICS (Note 1, 2, 3) (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		PIN	MIN	TYP	MAX	UNIT
Output Differential Voltage	$\|V_{OD}\|$	R_L=100Ω		OUT+ OUT-	300	400	500	mV
ΔV_{OD} Magnitude Change	ΔV_{OD}	(Figure 1 and Figure 2)				3	35	mV
Offset Voltage	V_{OS}	R_L=100Ω (Figure 1)			1.125	1.22	1.375	V
Offset Magnitude Change	ΔV_{OS}				0	1	25	mV
Power-off Leakage	I_{OFF}	V_{OUT}=3.6V or GND, V_{DD}=0V				±1	±10	μA
Output Short Circuit Current (Note 4)	I_{OS}	V_{OUT+} and V_{OUT-}=0V				-5	-24	mA
Differential Output Short Circuit Current (Note 4)	I_{OSD}	V_{OD}=0V				-4	-12	mA
Output Capacitance	C_{OUT}					3		pF
Input High Voltage	V_{IH}			TTL IN	2.0		V_{DD}	V
Input Low Voltage	V_{IL}				GND		0.8	V
Input High Current	I_{IH}	V_{IN}=3.3V or 2.4V				±2	±10	μA
Input Low Current	I_{IL}	V_{IN}=GND or 0.5V				±1	±10	μA
Input Clamp Voltage	V_{CL}	I_{CL}=-18mA			-1.5	-0.7		V
Input Capacitance	C_{IN}					3		pF
Power Supply Current	I_{DD}	No Load	V_{IN}=V_{DD} or GND	V_{DD}		3	8	mA
		R_L=100Ω				5	10	mA

Notes: 1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.
2. All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.
3. The **UDS90LV011** is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.
4. Output short circuit current (IOS) is specified as magnitude only, minus sign indicates direction only.

■ SWITCHING CHARACTERISTICS (Note 1, 2, 3, 4)

(V_{DD}=3.3V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Operating Frequency	f_{MAX}	R_L=100Ω, C_L=15pF (Figure 3 and Figure 4)	200	250		MHz
Differential Propagation Delay High to Low	t_{PHLD}		0.3	1.0	1.5	ns
Differential Propagation Delay Low to High	t_{PLHD}		0.3	1.1	1.5	ns
Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$	t_{SKD1}		0	0.1	0.7	ns
Differential Part to Part Skew (Note 6)	t_{SKD3}		0	0.2	1.0	ns
Differential Part to Part Skew (Note 7)	t_{SKD4}		0	0.4	1.2	ns
Transition Low to High Time	t_{TLH}		0.2	0.5	1.0	ns
Transition High to Low Time (Note 8)	t_{THL}		0.2	0.5	1.0	ns

Notes: 1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.

2. These parameters are specified by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
3. C_L includes probe and fixture capacitance.
4. Generator waveform for all tests unless otherwise specified: f = 1 MHz, ZO = 50Ω, tr ≤ 1 ns, tf ≤ 1 ns (10%-90%).
5. t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
6. t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
7. t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
8. f_{MAX} generator input conditions: tr = t_f < 1 ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45% / 55%, V_{OD} > 250mV. The parameter is specified by design. The limit is based on the statistical analysis of the device over the PVT range by the transitions times (t_{TLH} and t_{THL}).

■ PARAMETER MEASUREMENT INFORMATION

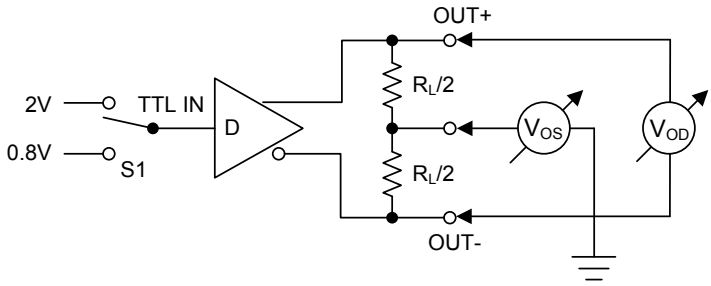


Figure 1. Differential Driver DC Test Circuit

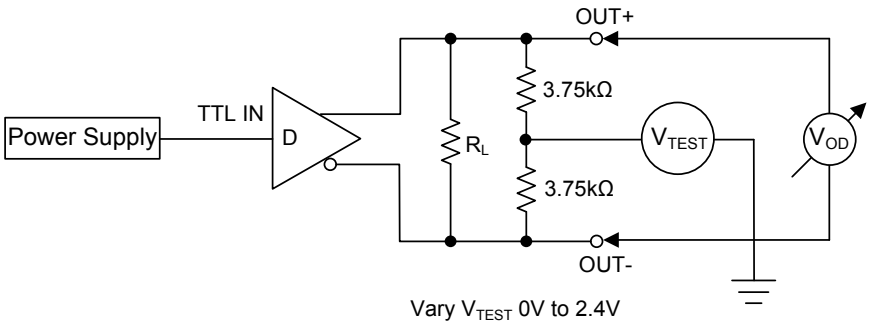


Figure 2. Differential Driver Full Load DC Test Circuit

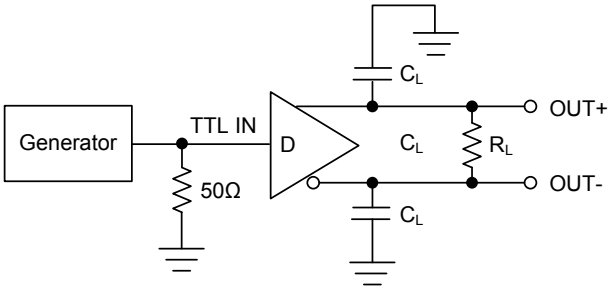


Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit

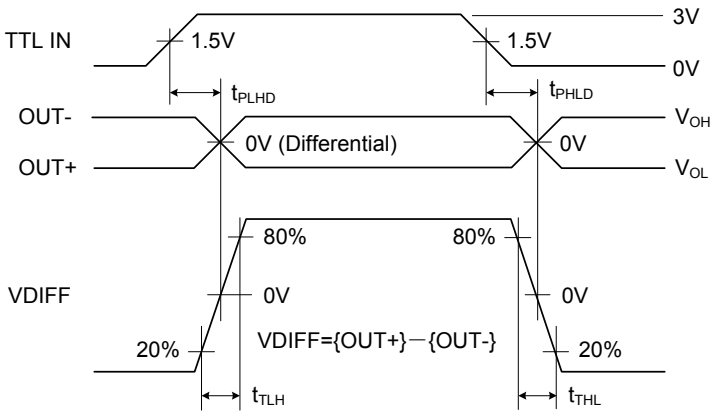


Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms