



## 4NM100

Preliminary

Power MOSFET

### 4.0A, 1000V N-CHANNEL SUPER-JUNCTION MOSFET

#### DESCRIPTION

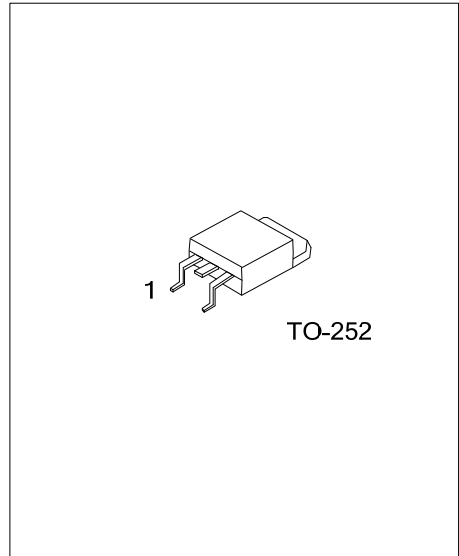
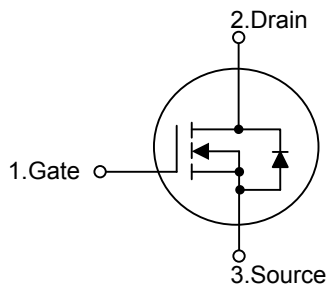
The UTC **4NM100** is an Super Junction MOSFET Structure. It uses UTC advanced planar stripe, DMOS technology to provide customers perfect switching performance, minimal on-state resistance.

The UTC **4NM100** is universally applied in electronic lamp ballasts based on half bridge topology, high efficiency switched mode power supplies, active power factor correction, etc.

#### FEATURES

- \*  $R_{DS(ON)} \leq 2.6 \Omega$  @  $V_{GS}=10V$ ,  $I_D=2.0A$
- \* High switching speed
- \* High breakdown voltage

#### SYMBOL



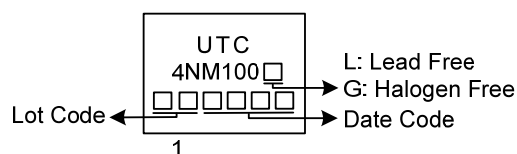
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4NM100L-TN3-R	4NM100G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

4NM100G-TN3-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	1000	V
Drain-Gate Voltage		$V_{DGR}$	1000	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	4	A
	Pulsed	$I_{DM}$	8	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	2.4	V/ns
Power Dissipation		$P_D$	25	W
Junction Temperature		$T_J$	$-55 \sim +150$	$^{\circ}\text{C}$
Storage Temperature Range		$T_{STG}$	$-55 \sim +150$	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3.  $I_{SD} \leq 4.0\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	$\theta_{JA}$	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	5 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

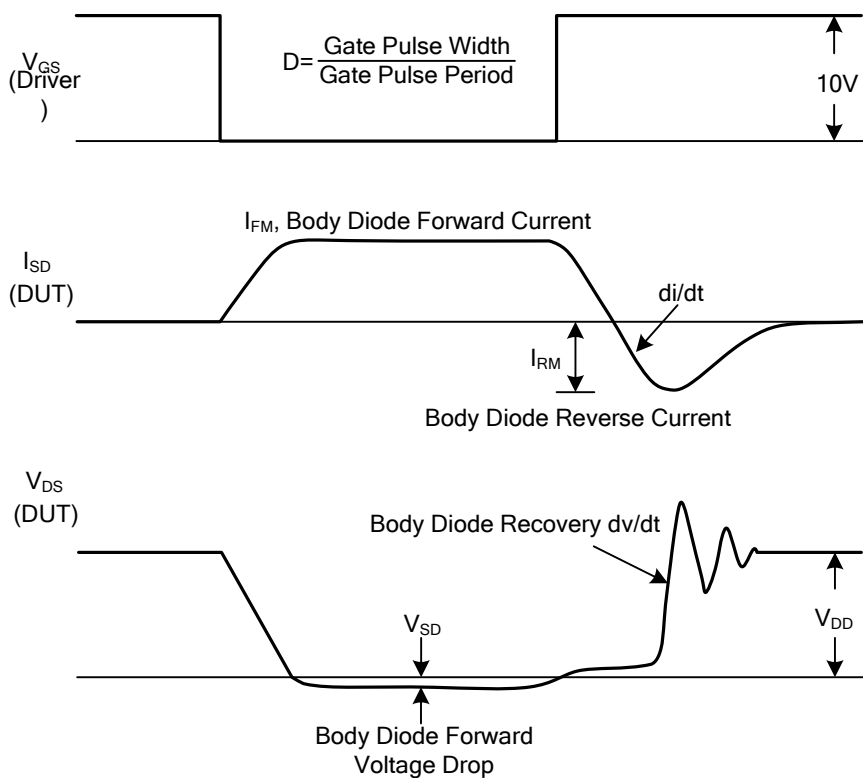
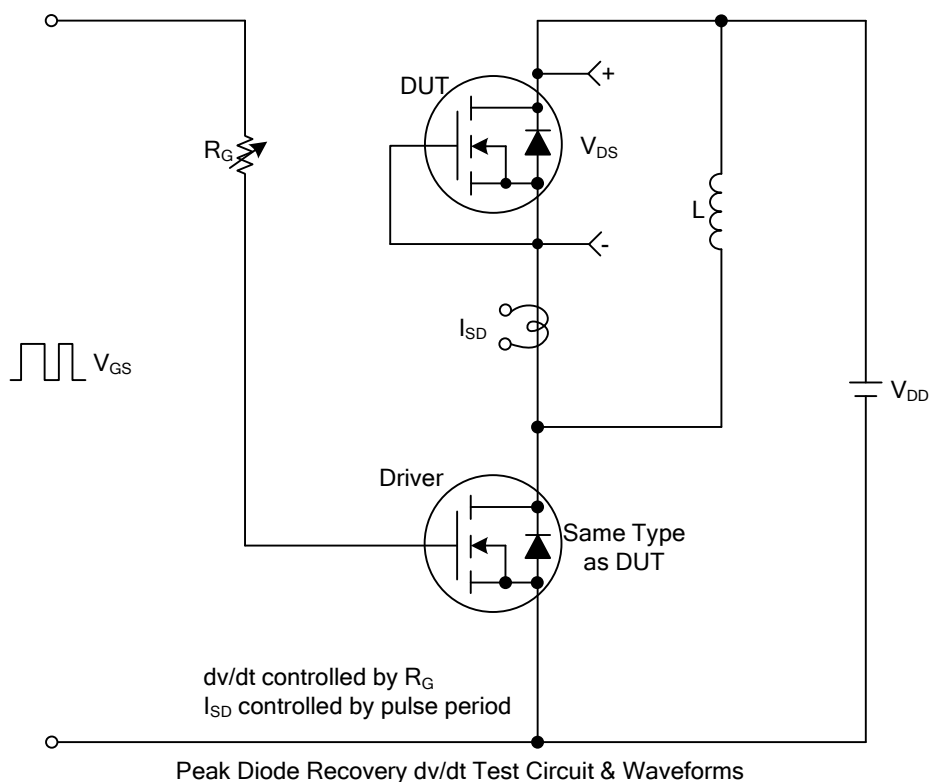
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	I <sub>D</sub> =0.25mA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	1000			V
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> =1000V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C			10	μA
			V <sub>DS</sub> =1000V, V <sub>GS</sub> =0V, T <sub>C</sub> =125°C			100	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub>	V <sub>GS</sub> =+30V, V <sub>DS</sub> =0V			+100	nA
	Reverse		V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2.0A			2.6	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz		350		pF
Output Capacitance		C <sub>OSS</sub>			110		pF
Reverse Transfer Capacitance		C <sub>RSS</sub>			6		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q <sub>G</sub>	V <sub>DS</sub> =800V, V <sub>GS</sub> =10V, I <sub>D</sub> =4.0A, (Note 1,2)		19		nC
Gate to Source Charge		Q <sub>GS</sub>			7		nC
Gate to Drain Charge		Q <sub>GD</sub>			5		nC
Turn-ON Delay Time		t <sub>D(ON)</sub>	V <sub>DD</sub> =100V, V <sub>GS</sub> =10V, I <sub>D</sub> =4.0A, R <sub>G</sub> =25Ω (Note 1,2)		6.4		ns
Rise Time		t <sub>R</sub>			17		ns
Turn-OFF Delay Time		t <sub>D(OFF)</sub>			43		ns
Fall-Time		t <sub>F</sub>			36		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I <sub>S</sub>	T <sub>C</sub> =25°C			4	A
Maximum Body-Diode Pulsed Current		I <sub>SM</sub>	T <sub>C</sub> =25°C			8	A
Drain-Source Diode Forward Voltage		V <sub>SD</sub>	I <sub>F</sub> =4.0A, V <sub>GS</sub> =0V			1.4	V
Reverse Recovery Time		t <sub>rr</sub>	I <sub>S</sub> =4.0A, V <sub>GS</sub> =0V,		468		ns
Reverse Recovery Charge		Q <sub>rr</sub>	dI <sub>F</sub> /dt=100A/μs (Note 1)		3.7		μC

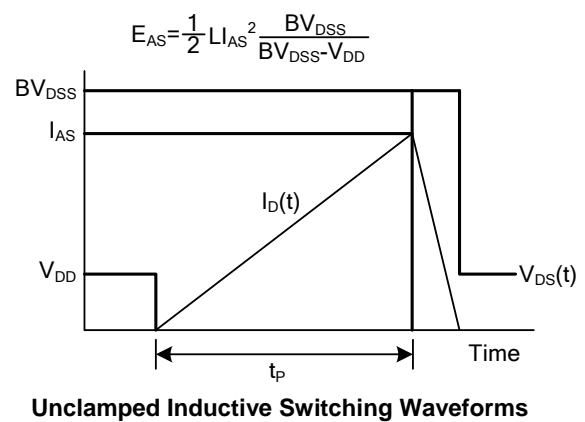
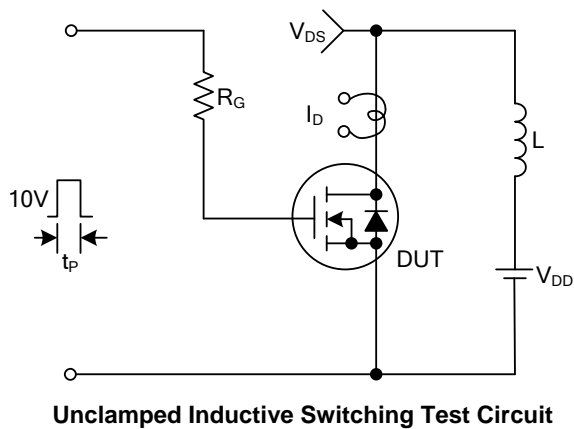
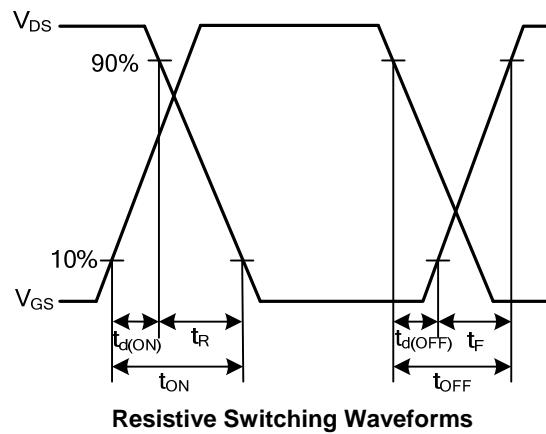
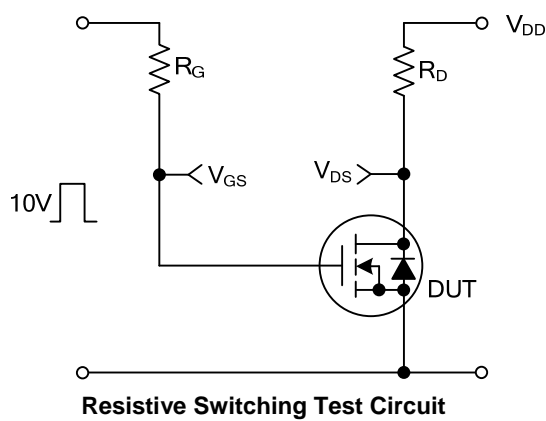
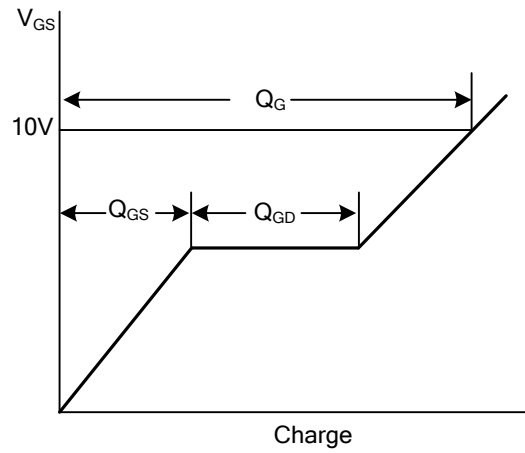
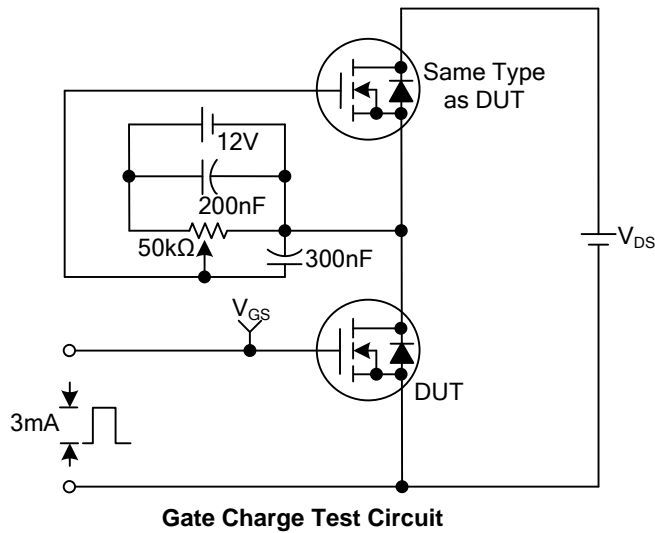
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

# ■ TEST CIRCUITS AND WAVEFORMS



# ■ TEST CIRCUITS AND WAVEFORMS(Cont.)



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