

**UT80N15H**

Preliminary

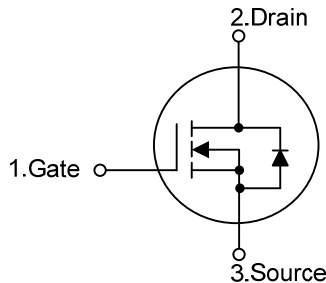
POWER MOSFET**80A, 150V N-CHANNEL
ENHANCEMENT MODE
TRENCH POWER MOSFET****■ DESCRIPTION**

The UTC **UT80N15H** is a N-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with ideal for low voltage inverter applications.

The UTC **UT80N15H** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

■ FEATURES

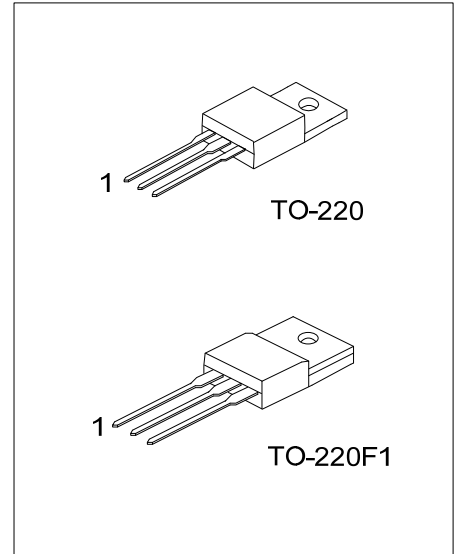
- * $R_{DS(ON)} \leq 13 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=40\text{A}$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

■ SYMBOL**■ ORDERING INFORMATION**

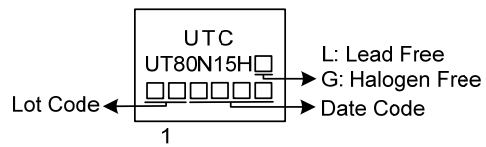
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT80N15HL-TA3-T	UT80N15HG-TA3-T	TO-220	G	D	S	Tube
UT80N15HL-TF1-T	UT80N15HG-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UT80N15HG-TA3-T		(1) Packing Type	(1) T: Tube
		(2) Package Type	(2) TA3: TO-220, TF1: TO-220F1
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	150	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	80	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	160	A
Avalanche energy	Single Pulsed (Note 3)	E_{AS}	291	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6.5	V/nS
Power Dissipation	TO-220	P_D	250	W
	TO-220F1		48	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=76.3\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^{\circ}\text{C}$.

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	0.5	$^{\circ}\text{C}/\text{W}$
	TO-220F1		2.6	$^{\circ}\text{C}/\text{W}$

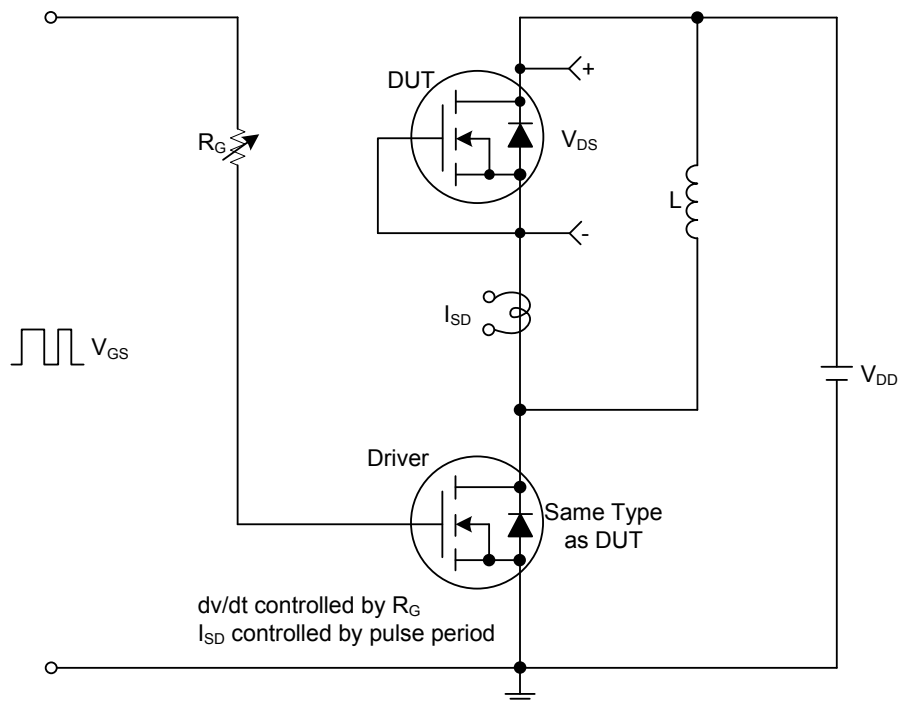
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	150			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =150V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =40A			13	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		17.3		nF
Output Capacitance		C _{OSS}			665		pF
Reverse Transfer Capacitance		C _{RSS}			570		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =120V, V _{GS} =10V, I _D =80A, (Note 1, 2)		350		nC
Gate to Source Charge		Q _{GS}			80		nC
Gate to Drain Charge		Q _{GD}			120		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DD} =75V, V _{GS} =10V, I _D =80A, R _G =3.3Ω (Note 1, 2)		50		ns
Rise Time		t _R			30		ns
Turn-off Delay Time		t _{D(OFF)}			160		ns
Fall-Time		t _F			54		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				80	A
Maximum Body-Diode Pulsed Current		I _{SM}				160	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =80A, V _{GS} =0V			1.3	V
Reverse recovery time (Note 1)		t _{rr}	I _S =30A, V _{GS} =0V,		86		ns
Reverse recovery charge		Q _{rr}	dl _F /dt = 100A/μs		281		nC

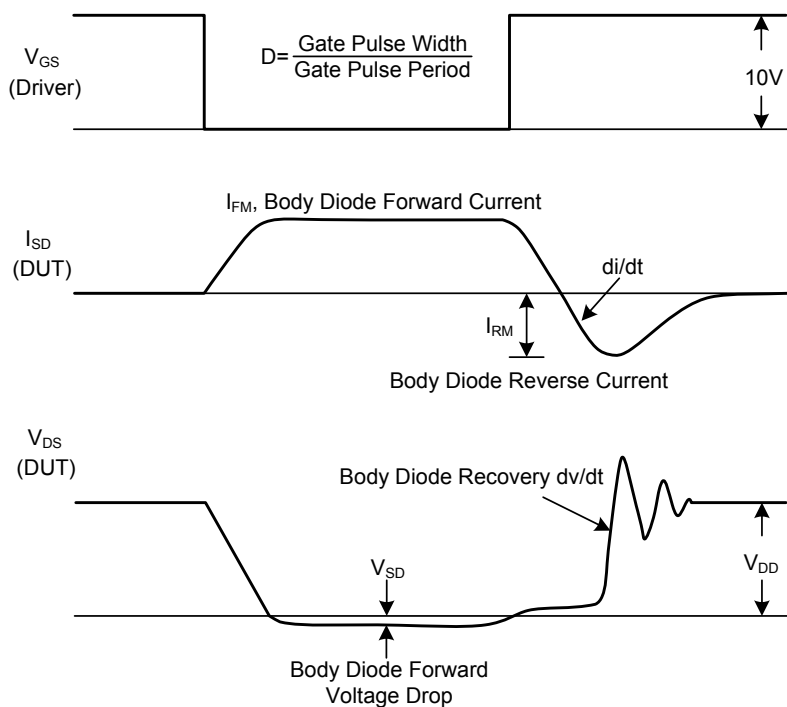
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



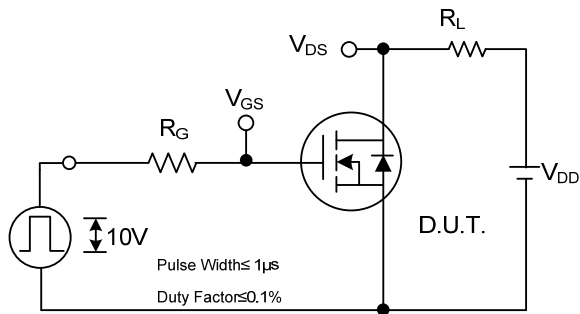
Peak Diode Recovery dv/dt Test Circuit



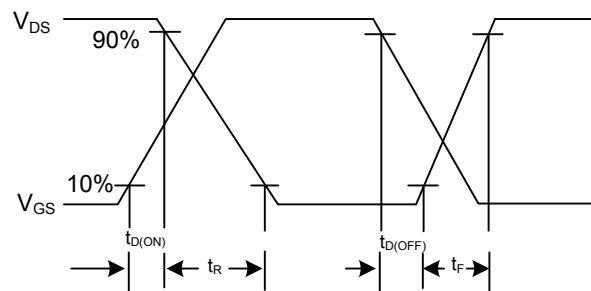
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

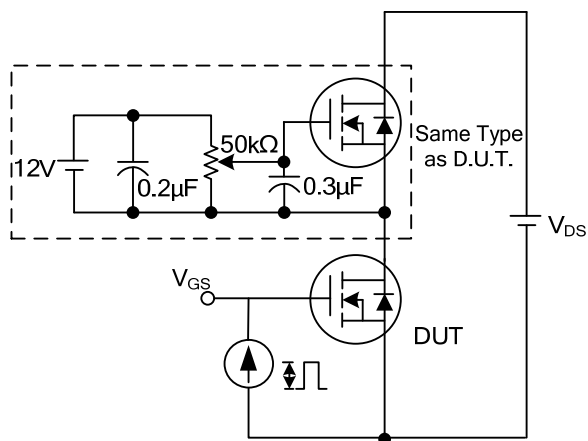
■ TEST CIRCUITS AND WAVEFORMS



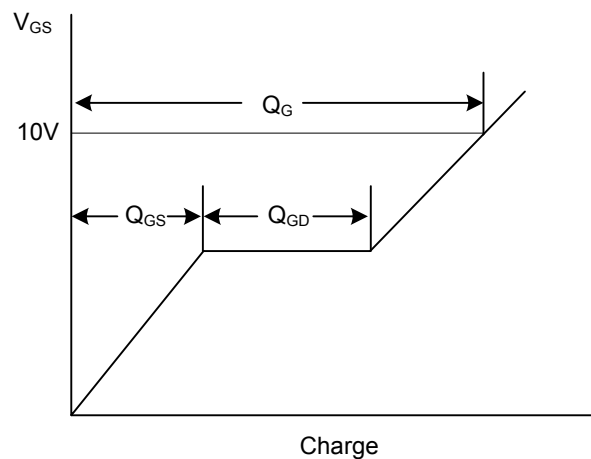
Switching Test Circuit



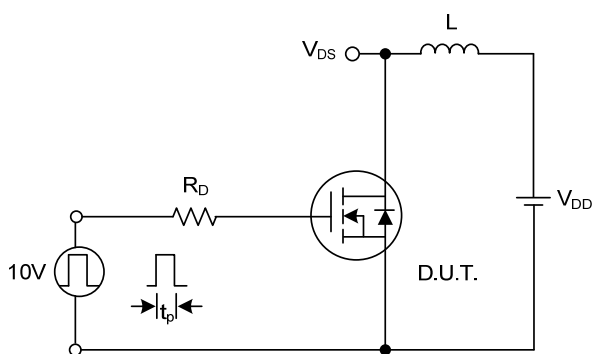
Switching Waveforms



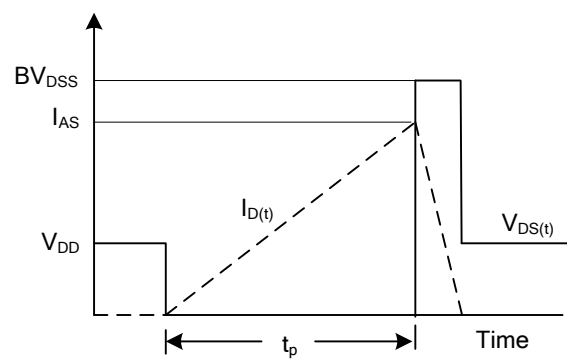
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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