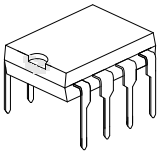
LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS



DIP-8

■ DESCRIPTION

The UTC **USQ6502** provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, and switch to valley switching at light load.

The UTC **USQ6502** is a high performance current mode PWM controller ideally suited for low standby power. Drain-start up cell is design to minimize the standby power to minimize the standby power. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition.

The UTC **USQ6502** contains protection with automatic recovery including OLP (over load protection), OCP (cycle-by-cycle current limiting), and UVLO (V_{DD} over voltage clamp and under voltage lockout). It also provides the protections including OTP (over temperature protection), BNO(AC Brown Out protection) , LNO(AC Over voltage protection), OVP (V_{CC} or DC output over voltage protection) with automatic recovery. To protect the power MOSFET, Gate-drive output is fixed up to 16V max.

The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch, which offering minima external component count in the design. Excellent EMI performance is achieved with UTC proprietary frequency hopping technique (ZL201020615247.1) together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation.

UTC **USQ6502** is packaged by using tiny DIP-8 package. It has such applications as: battery charger, power adaptor, set-top box power supplies, ink jet printers, open-frame SMPS.

■ FEATURES

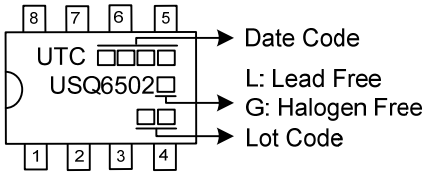
* Proprietary frequency hopping for Improved EMI performance
* Low standby power with only 30~70mw
* Cycle-by-cycle current limiting
* CCM/Valley Switching Operation
* Fixed switch frequency 65~85kHz
* Dynamic peak current limiting for constant output power
* Built-in synchronized slope compensation
* Gate output voltage clamped at 16V
* Adjustable DC output OVP
* OLP/V_{CC} OVP/OTP/BNO/LNO (automatic recovery)
* Internal Soft Start

■ ORDERING INFORMATION

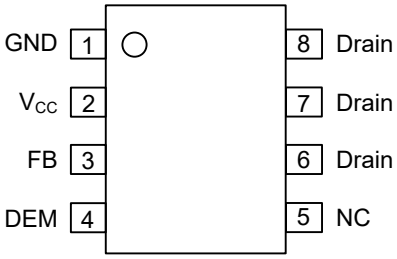
Ordering Number		Package	Packing
Lead Free	Halogen Free		
USQ6502L-D08-T	USQ6502G-D08-T	DIP-8	Tube

USQ6502G-D08-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) D08: DIP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



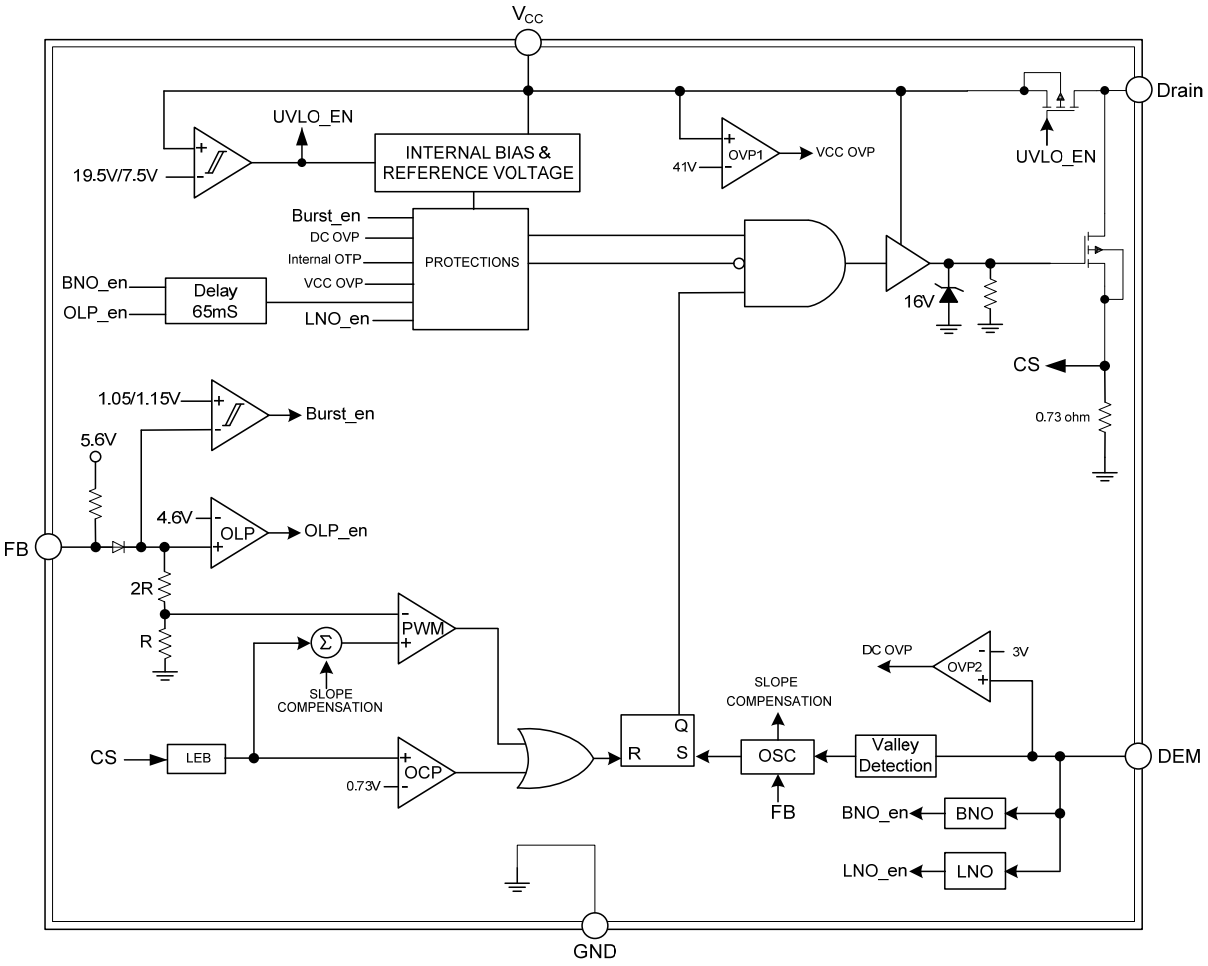
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground.
2	V_{CC}	IC power supply pin.
3	FB	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is generated by this pin voltage.
4	DEM	Transformer core demagnetization detection pin. This pin is also used for output over voltage protection (Output OVP).
5	NC	No Connection.
6, 7, 8	Drain	High voltage power MOSFET drain connection.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.3 ~ 45	V
FB, CS, DEM		-0.3 ~ 6	V
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	9.5 ~ 38	V
Start up Charge Current to CV$_{CC}$	I_{CH}	≥ 0.5	mA
V_{CC} Capacitor		4.7 ~ 68	μF
Open Frame Output Power for 85~264VAC	P_{O_MAX}	20	W

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	250	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{CC}=15V, T_A=+25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{CC} (ON)			17.5	19.5	21.5	V
V_{CC} (OFF)			6.5	7.5	8.5	V
Startup Current		VCC<VCC (ON)-0.5V		2	15	μA
Operating Current		V_{FB}=3V		0.8		mA
		V_{FB}=Burst Level		0.25		mA
V_{CC} OVP Threshold			39	41	43	V
OSCILLATOR & SWITCHING FREQUENCY						
Switching Frequency			60	65	70	KHz
Temperature Stability		Guaranteed by Design			10	%
Voltage Stability					10	%
Green Mode Frequency			20			KHz
Frequency Spreading Range			+9		-9	%
Max.Duty Cycle	DC_{MAX}	V_{FB} =3.9V	58	64	70	%
VOLTAGE FEEDBACK						
Open Loop Voltage			4.9		5.8	V
OLP Level				4.6		V
OLP De-Bounce Time		V_{FB}>4V	45	65	95	mS
Burst-Mode Enter FB Voltage	V_{FB-IN}			1.05		V
Burst-Mode Quit FB Voltage	V_{FB-OUT}			1.15		V
FB Pin Short Current	I_{FB_SHORT}			120		μA
CURRENT SENSING						
Peak Current Flat Threshold Voltage		Guaranteed by Design		1		A
Peak Current Valley Threshold			0.61	0.67	0.73	A
Lead Edge Blanking Time	T_{LEB}	Guaranteed by Design		350		ns
Soft Start Time				10		mS

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER MOS-TRANSISTOR SECTION						
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS}=0V, I_D=250μA	650			V
Turn-On Voltage between Gate and Source	V_{TH}	V_{DS}=V_{GS}, I_D=250μA	2		4	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=0.8A		2		Ω
DEMAGNETIZATION (DEM) DETECTION						
DEM OVP Sampling Instant		Guaranteed by Design		3		μS
DEM OVP Threshold Level			2.8	3	3.2	V
DEM OVP De-Bounce Time		Guaranteed by Design		7		Times
Demagnetization Detection Level		Guaranteed by Design		220		mV
Demagnetization Delay		Guaranteed by Design		200		nS
DEM_BNI		Guaranteed by Design	95	105	110	μA
DEM_BNO			90	95	100	μA
BNO De-Bounce Time			45	65	95	mS
DEM_LNO		Guaranteed by Design	405	427	450	μA
THERMAL SHUT DOWN						
OTP Threshold				150		°C

■ APPLICATION NOTE

The UTC **USQ6502** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **USQ6502** series.

Start-up

HV-start up cell charge to V_{CC} capacitor during V_{CC} on, and HV-start up cell is shutdwon when V_{CC} voltage is over V_{CCON} threshold. So standby power is only 30~70mw. The D1 IN4148 can improve surge capability to 6.6KV.

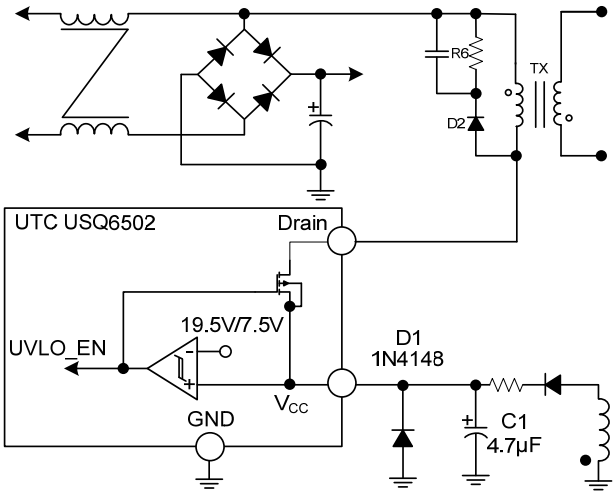


Fig. 1 Startup Circuit

Operation Mode

The UTC **USQ6502** provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, once if the converter enters into DCM, the UTC **USQ6502** automatically finds the local minimum V_{DS} point and switching at this local valley.

Normally, the conduction loss is dominated at heavy load condition, and the switching loss turns to be larger than conduction loss in light load, especially at 1/4 ~ 1/2 of full load. By this kind of mixed mode operation to have CCM in heavy load and valley switching in light load can optimize the overall average efficiency during the entire operation range.

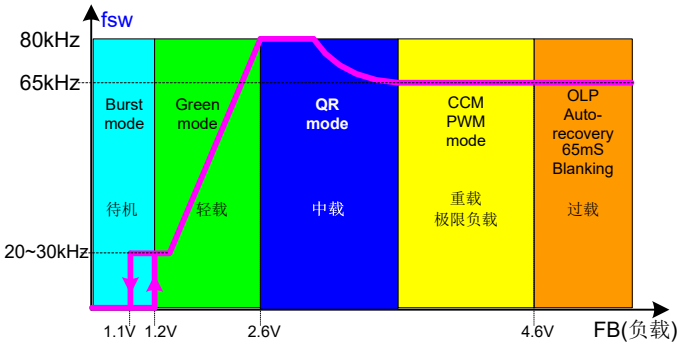


Fig. 2 FB vs. Fsw Curve

■ APPLICATION NOTE (Cont.)

As shown in Fig. 3, at deep light-load or no-load condition, the switching loss is the dominant factor. To improve the light-load efficiency, burst mode operation will stop the switching cycle of the OUT pin when FB pin voltage is below "V_{FB_IN}" Level and restart the switching cycle of the OUT pin when FB pin voltage is above "V_{FB_OUT}".

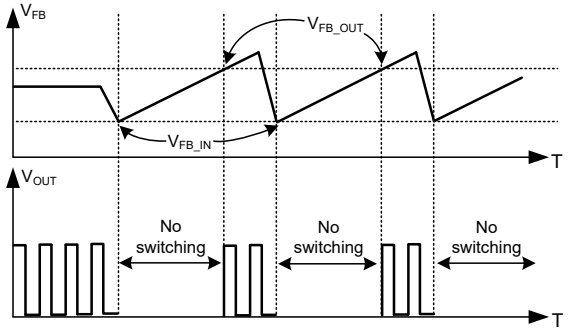


Fig. 3 Burst Mode Operation

Over Voltage Protection on VCC Pin (V_{CC} OVP)

The V_{CC} OVP will shut down the switching of the power MOSFET whenever V_{DD} >V_{OVP}. The OVP event as followed Fig.4.

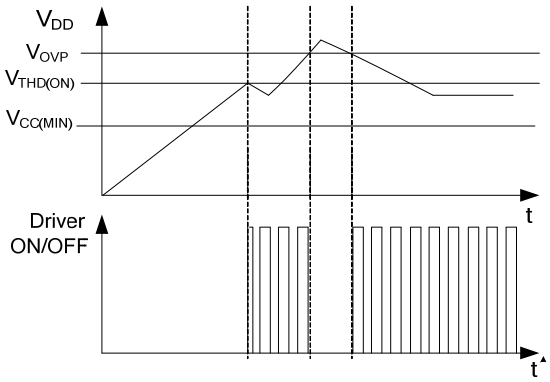


Fig.4 OVP case

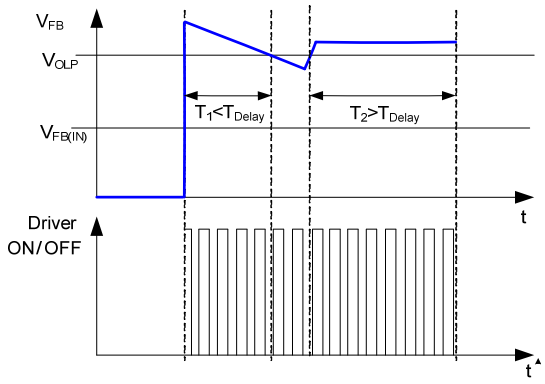


Fig.5 OLP case

Over Load &Open Loop & Output Short Protection (OLP or OSP)

OLP or OSP will shut down driver when V_{FB}> V_{OLP} for continual a blanking time. The OLP or OSP event as followed Fig.5.

Over Temperature Protection (OTP)

OTP will shut down driver when the NTC resistor temperature T_J>$T_{(THR)}$.

Brown in/out & DEM OVP Protection

To prevent high current stress at too low AC voltage condition, the UTC **USQ6502** implements an AC brown in/out protection through the DEM pin. The current sourcing out from the DEM pin when the OUT pin is enabled is monitored to have the AC input voltage level information. When the current keeps above the DEM_BNI threshold (105μA, typ.) for more than BNI De-bounce time 7 cycles, the AC brown in condition is issued and the OUT is enabled. Once if the current keeps under the DEM_BNO threshold (95μA, typ.) for more than BNO De-bounce time, the AC brown out condition is issued and the OUT is disabled.

The equation is used to calculate the brown in/out level:

$$V_{AC\_BNI} = I_{BNI} \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}} \quad , \quad V_{AC\_BNO} = I_{BNO} \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}}$$

■ APPLICATION NOTE (Cont.)

An over voltage protection for Vo is fulfilled by sampling the voltage on the DEM waveform after OUT is turn-off. After a short delay after OUT off, the sampled voltage is compared to the internal over voltage reference is determined whether if an OVP event is occurred. The internal over voltage reference is biased at 3V, uses can define the resistor divider ratio by the equation below based on the desired OVP level:

$$V_{O\_OVP} = V_{DEM\_OVP} \times \frac{R_{DEM\_U} + R_{DEM\_D}}{R_{DEM\_D}} \times \frac{N_{SEC}}{N_{AUX}}$$

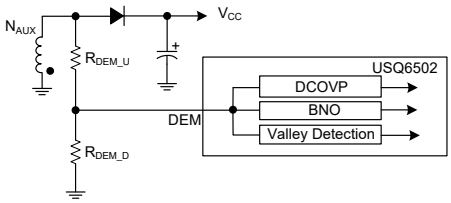


Fig. 6 DEM-Pin Divider

Cycle by Cycle Over-Current Protection (OCP)

In a Flyback topology converter, the main MOSFET switch of the Flyback converter turns on and off rapidly. The energy is stored in the inductor when the MOSFET turns on. The inductor current flowing through the sensing resistor (R_{CS}) is shown in Fig.7. The current limit is determined by the equation below:

$$I_{PEAK} = 1A$$

In order to prevent the CS pin from false triggering, an internal leading edge blanking time (350nS Typ.) is added.

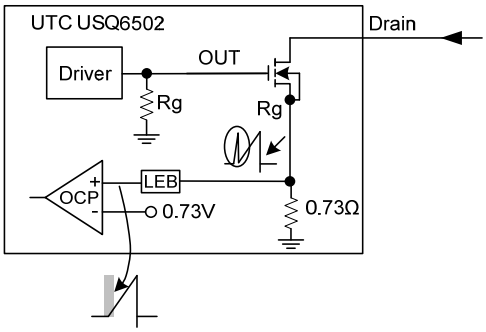


Fig. 7 Current Sensing

■ TYPICAL APPLICATION CIRCUIT