



UTR040N03M

Preliminary

Power MOSFET

100A, 30V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

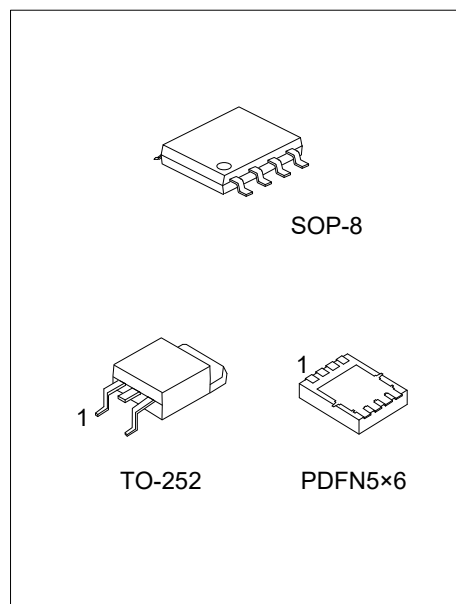
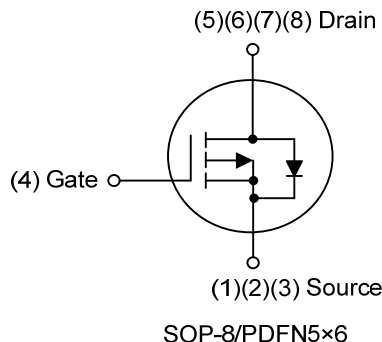
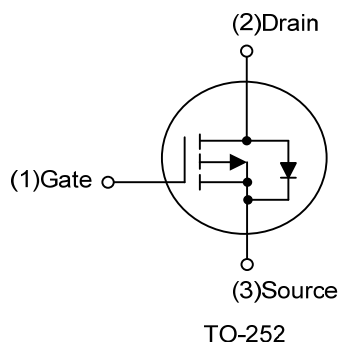
DESCRIPTION

The UTC **UTR040N03M** uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

FEATURES

- * For TO-252/ PDFN5×6
 $R_{DS(ON)} \leq 4.0 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=40\text{A}$
- * For SOP-8
 $R_{DS(ON)} \leq 4.0 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
- * For TO-252/ PDFN5×6/SOP-8
 $R_{DS(ON)} \leq 7.0 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=20\text{A}$
- * High density cell design for ultra low $R_{DS(ON)}$
- * Fully characterized avalanche voltage and current
- * Good stability and uniformity with high EAS
- * Excellent package for good heat dissipation

SYMBOL



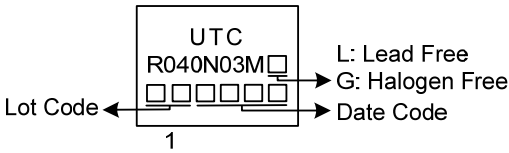
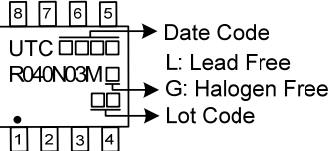
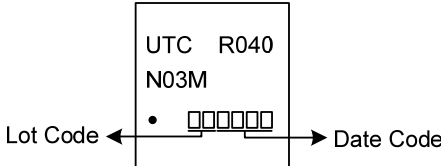
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTR040N03ML-TN3-R	UTR040N03MG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UTR040N03ML-S08-R	UTR040N03MG-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UTR040N03ML-P5060-R	UTR040N03MG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTR040N03MG-TN3-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) TN3: TO-252, S08: SOP-8, P5060: PDFN5×6
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

PACKAGE	MARKING
TO-252	 Diagram showing marking on a TO-252 package. The marking includes 'UTC', 'R040N03M', and a date code '1'. Arrows indicate the Lot Code (left) and Date Code (right). Legend: L: Lead Free, G: Halogen Free.
SOP-8	 Diagram showing marking on an SOP-8 package. The marking includes 'UTC', 'R040N03M', and a date code '1'. Arrows indicate the Lot Code (left) and Date Code (right). Legend: L: Lead Free, G: Halogen Free.
PDFN5x6	 Diagram showing marking on a PDFN5x6 package. The marking includes 'UTC', 'R040', 'N03M', and a date code '1'. Arrows indicate the Lot Code (left) and Date Code (right).

■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Drain Current	Continuous	TO-252/PDFN5X6	I _D	100	A
		SOP-8		17	
	Pulsed (Note 2)	TO-252/PDFN5X6	I _{DM}	200	A
		SOP-8		140	
Single Pulsed Avalanche Energy (Note 3)			E _{AS}	133	mJ
Peak Diode Recovery dv/dt (Note 4)			dv/dt	3.9	V/ns
Power Dissipation	TO-252		P _D	58	W
	SOP-8			2.2	W
	PDFN5×6			45	W
Junction Temperature			T _J	+150	°C
Storage Temperature			T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 51.6\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J \leq T_{JMAX}$, $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
	SOP-8		90	$^{\circ}\text{C}/\text{W}$
	PDFN5×6		65	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-252	θ_{JC}	2.16	$^{\circ}\text{C}/\text{W}$
	SOP-8		56	$^{\circ}\text{C}/\text{W}$
	PDFN5×6		2.77	$^{\circ}\text{C}/\text{W}$

Notes: 1. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

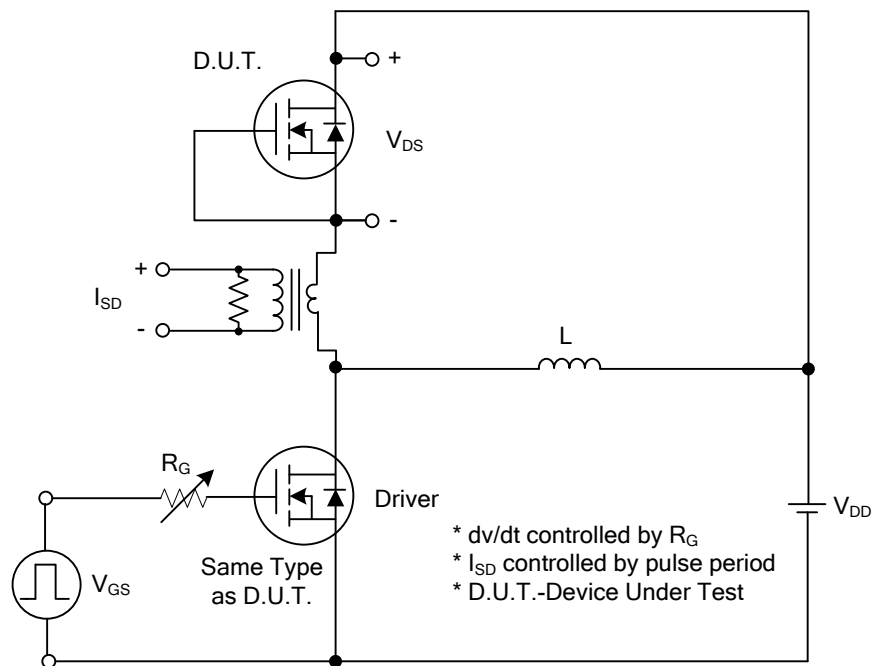
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	TO-252 PDFN5x6	R _{DS(ON)}	V _{GS} =10V, I _D =40A			4.0	mΩ
	SOP-8		V _{GS} =10V, I _D =20A				
Static Drain-Source On-State Resistance			V _{GS} =4.5V, I _D =20A			7.0	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =15V, V _{GS} =0V, f=1.0MHz		2910		pF
Output Capacitance		C _{OSS}			480		pF
Reverse Transfer Capacitance		C _{RSS}			350		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =24V, V _{GS} =10V, I _D =100A		78		nC
Gate to Source Charge		Q _{GS}			15		nC
Gate to Drain Charge		Q _{GD}			18		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =15V, V _{GS} =10V, I _D =100A, R _G =3Ω		12		ns
Rise Time		t _R			17		ns
Turn-OFF Delay Time		t _{D(OFF)}			52		ns
Fall-Time		t _F			30		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V _{SD}	I _{SD} =20A			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =30A, dI/dt=100A/μs		75		ns
Body Diode Reverse Recovery Charge		Q _{rr}			64		nC

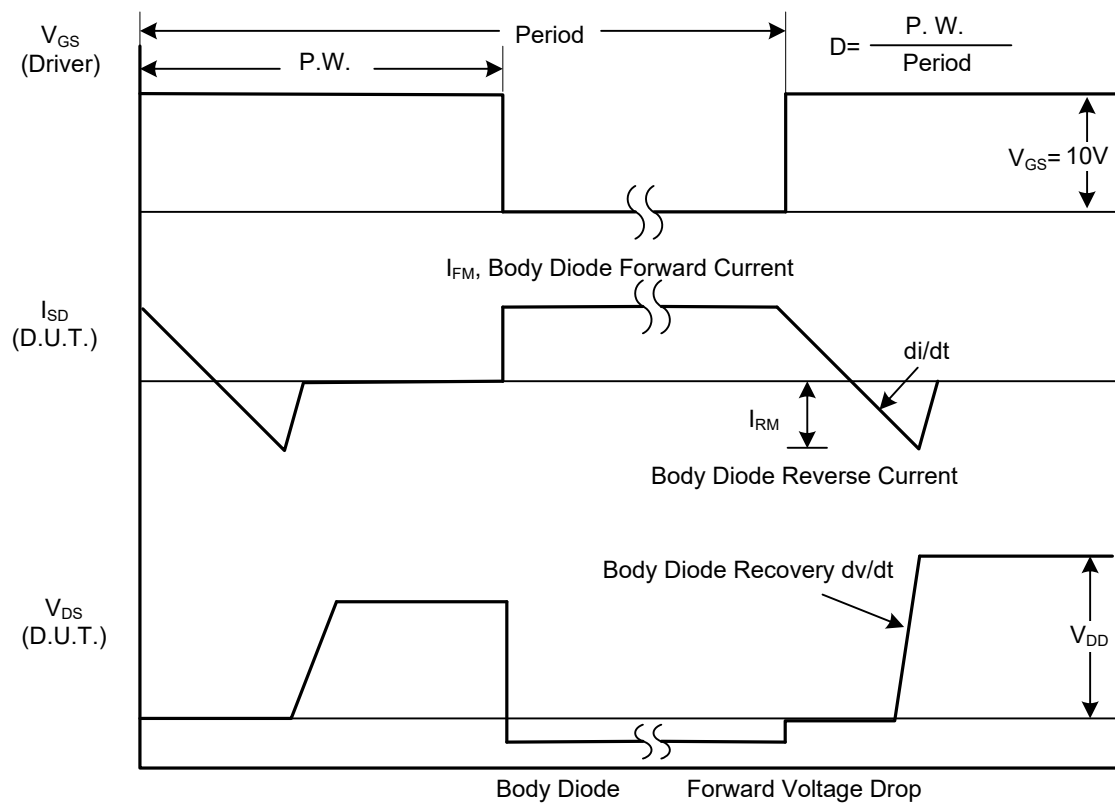
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

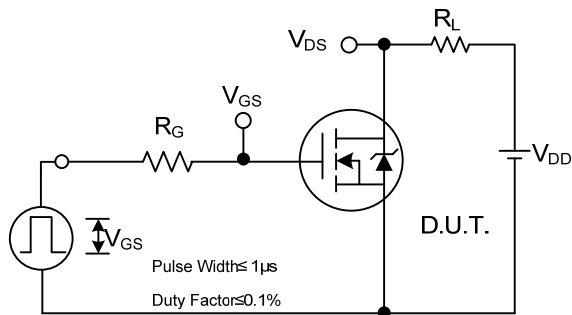


Peak Diode Recovery dv/dt Test Circuit

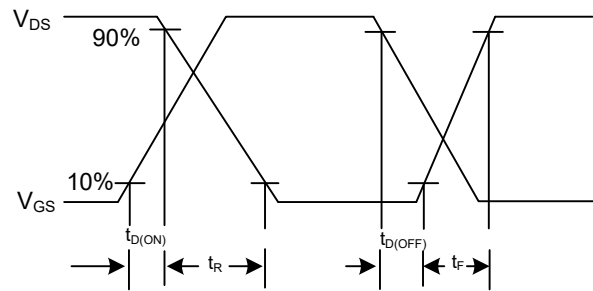


Peak Diode Recovery dv/dt Waveforms

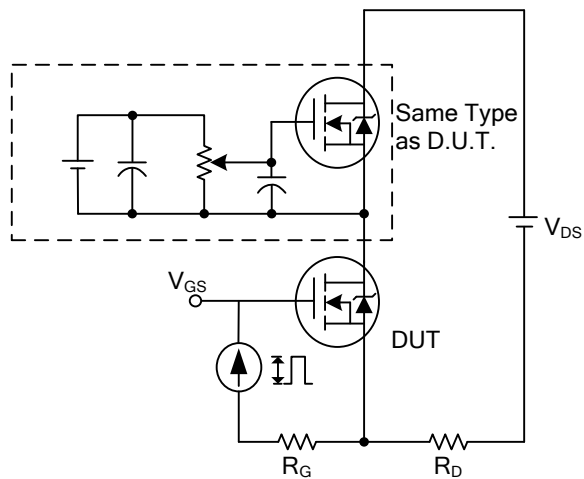
■ TEST CIRCUITS AND WAVEFORMS



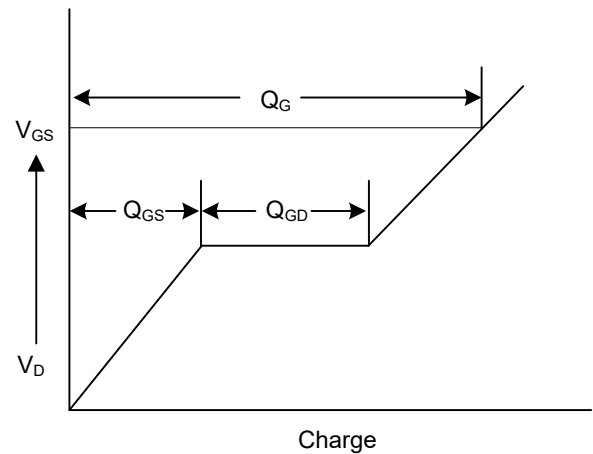
Switching Test Circuit



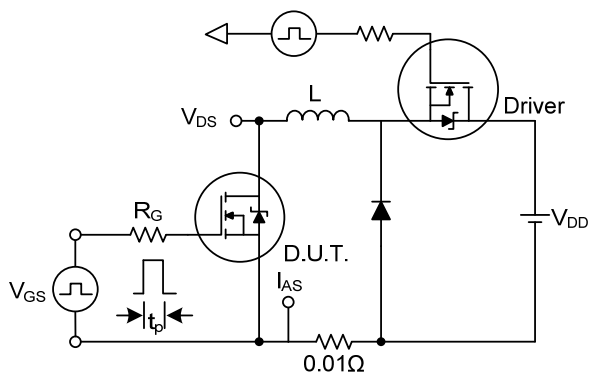
Switching Waveforms



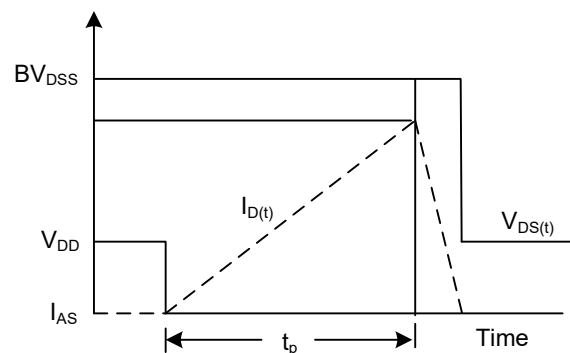
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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