

**USG80N15H**

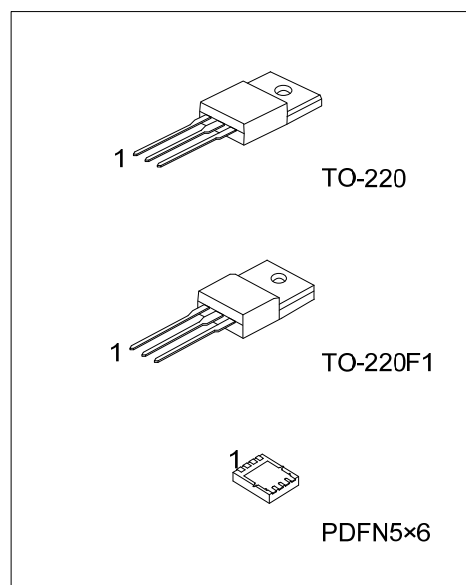
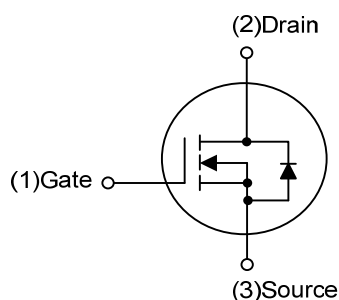
Preliminary

POWER MOSFET**80A, 150V N-CHANNEL SGT
ENHANCEMENT POWER
MOSFET****DESCRIPTION**

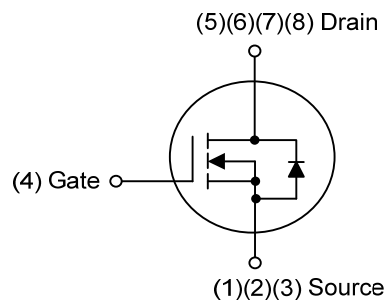
The UTC **USG80N15H** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

FEATURES

- * $R_{DS(ON)} \leq 13.5 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=40\text{A}$
- * Extremely low on-resistance $R_{DS(ON)}$
- * Excellent Low Ciss

**SYMBOL**

TO-220/TO-220F1



PDFN5x6

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
USG80N15HL-TA3-T	USG80N15HG-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
USG80N15HL-TF1-T	USG80N15HG-TF1-T	TO-220F1	G	D	S	-	-	-	-	-	Tape Reel
USG80N15HL-P5060-R	USG80N15HG-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

USG80N15HG-TA3-T		(1) Packing Type	(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TF1: TO-220F1, P5060: PDFN5x6 (3) G: Halogen Free and Lead Free, L: Lead Free
		(2) Package Type	
		(3) Green Package	

■ MARKING

TO-220 / TO-252	PDFN5×6
UTC USG80N15H □ Lot Code ← □ □ □ □ □ → Date Code L: Lead Free G: Halogen Free 1	UTC USG 80N15H Lot Code ← • □ □ □ □ □ → Date Code

■ **ABSOLUTE MAXIMUM RATING** ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	DC	I_D	80	A
	Pulsed (Note 2)	I_{DM}	160	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	92	mJ
Power Dissipation	TO-220	P_D	150	W
	TO-220F1		36	W
	PDFN5×6		100	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=43\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$.

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F1	θ_{JA}	62.5	$^{\circ}\text{C/W}$
	PDFN5×6		65(Note)	$^{\circ}\text{C/W}$
Junction to Case	TO-220	θ_{JC}	0.83	$^{\circ}\text{C/W}$
	TO-220F1		3.47(Note)	$^{\circ}\text{C/W}$
	PDFN5×6		1.25(Note)	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

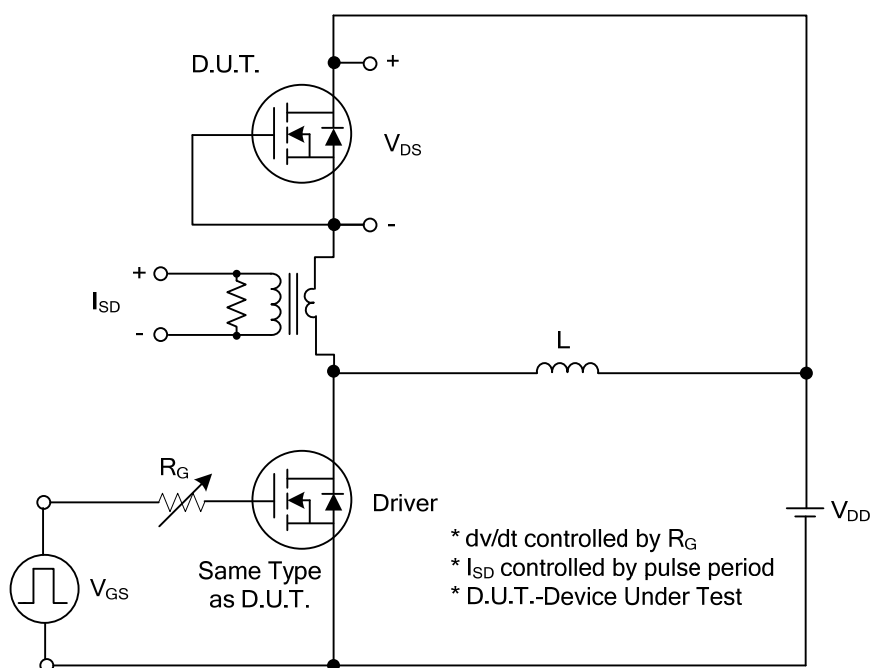
■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	150			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =150V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =40A			13.5	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1.0MHz		1300		pF
Output Capacitance		C _{OSS}			485		pF
Reverse Transfer Capacitance		C _{RSS}			13		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =120V, V _{GS} =10V, I _D =80A (Note 1, 2)		27		nC
Gate to Source Charge		Q _{GS}			12		nC
Gate to Drain Charge		Q _{GD}			7		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =75V, V _{GS} =10V, I _D =80A, R _G =3Ω (Note 1, 2)		12		ns
Rise Time		t _R			16		ns
Turn-OFF Delay Time		t _{D(OFF)}			18		ns
Fall-Time		t _F			15		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				80	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				160	A
Diode Forward Voltage		V _{SD}	I _F =80A, V _{GS} =0V			1.4	V

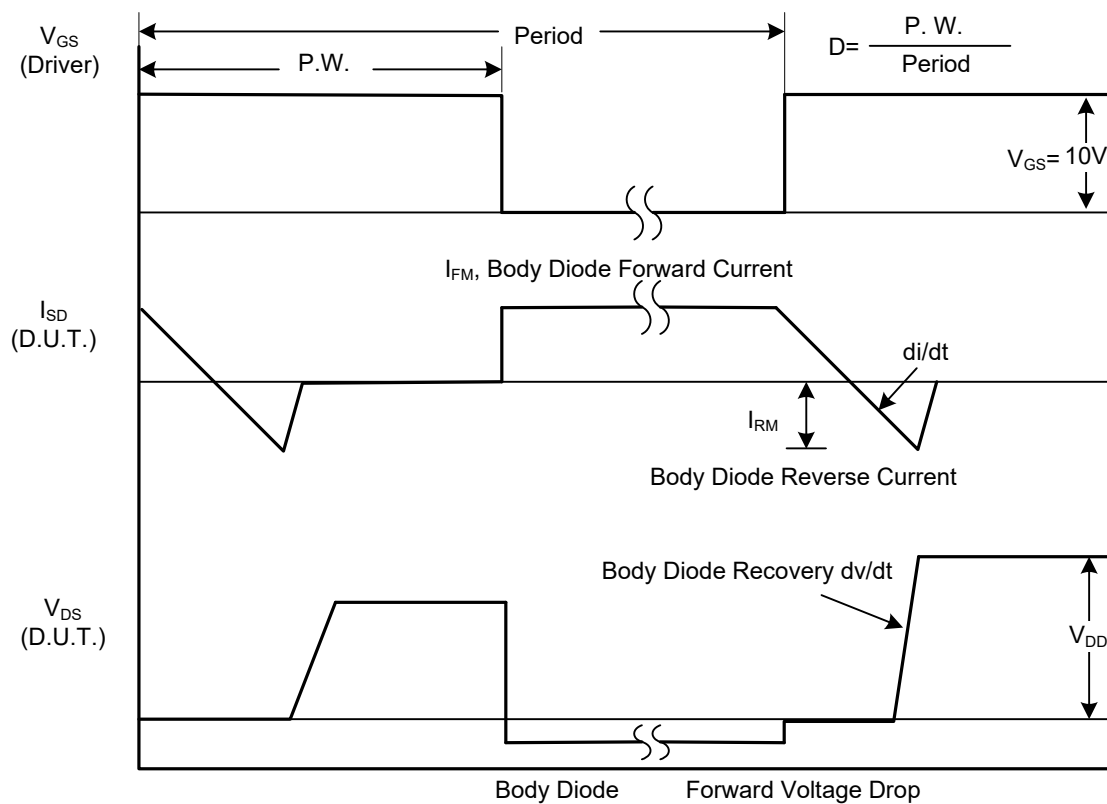
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

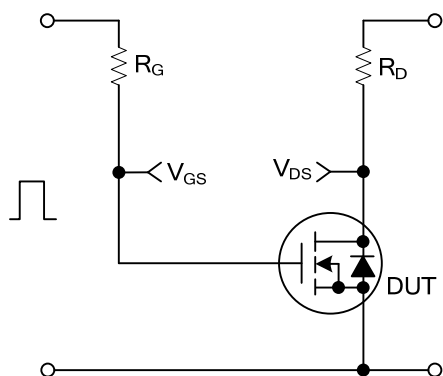


Peak Diode Recovery dv/dt Test Circuit

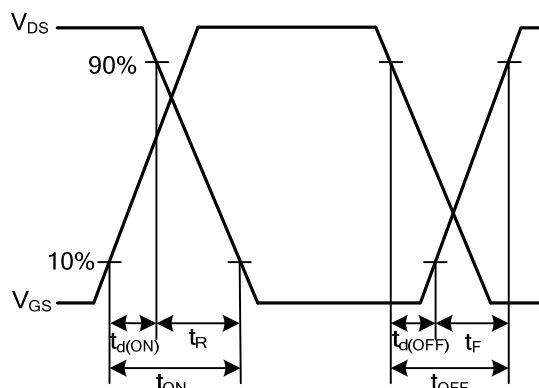


Peak Diode Recovery dv/dt Waveforms

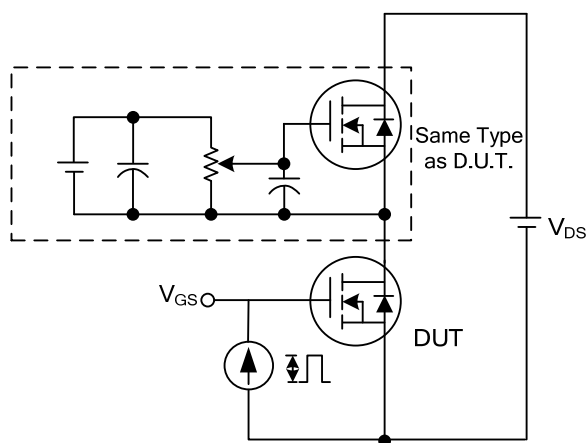
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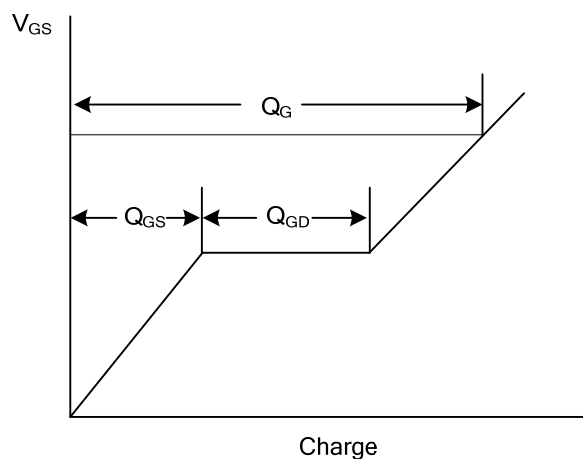
Switching Test Circuit



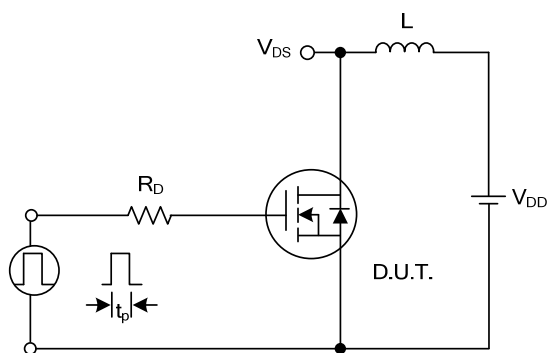
Switching Waveforms



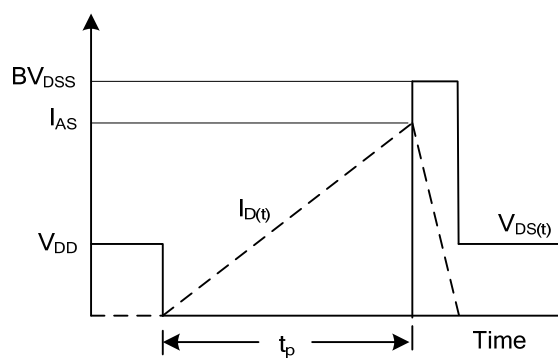
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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