

**UT8PP06**

Preliminary

Power MOSFET

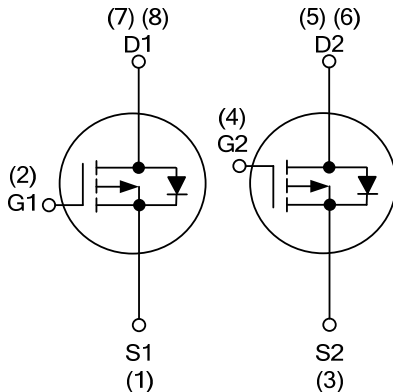
**P-CHANNEL ENHANCEMENT
MODE POWER MOSFET****DESCRIPTION**

The UTC **UT8PP06** is a P-channel MOS Field Effect Transistor. it uses UTC's advanced technology to provide the customers with high switching speed and a minimum on-state resistance.

The UTC **UT8PP06** is suitable for high voltage switching applications.

FEATURES

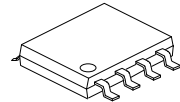
- * $R_{DS(ON)} \leq 98 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -4.0\text{A}$
- * $R_{DS(ON)} \leq 140 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -3.0\text{A}$
- * Low capacitance
- * Low gate charge
- * Fast switching capability
- * Avalanche energy specified

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT8PP06L-S08-R	UT8PP06G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

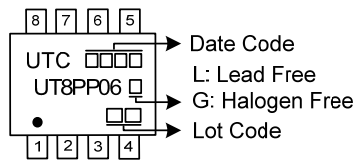
Note: Pin Assignment: G: Gate D: Drain S: Source

UT8PP06G-S08-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) S08: SOP-8
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



SOP-8

■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-8	A
Pulsed Drain Current (Note 2)	I_{DM}	-16	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	8
Peak Diode Recovery dv/dt (Note 4)	dv/dt	2.6	V/ns
Power Dissipation	P_D	1.2	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = -13\text{A}$, $V_{DD} = -50\text{V}$, $R_G = 25\ \Omega$ Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -8.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	125	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	104	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	-60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V			-1	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
Cutoff Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-4.0A			98	mΩ
		V _{GS} =-4.5V, I _D =-3.0A			140	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =-25V, V _{GS} =0V, f=1.0MHz		770		pF
Output Capacitance	C _{OSS}			65		pF
Reverse Transfer Capacitance	C _{RSS}			48		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =-48V, V _{GS} =-10V, I _D =-8.0A,		18		nC
Gate to Source Charge	Q _{GS}			4.5		nC
Gate to Drain Charge	Q _{GD}			2.5		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DS} =-30V, V _{GS} =-10V, I _D =-8.0A, R _G =3Ω		5		ns
Rise Time	t _R			16		ns
Turn-OFF Delay Time	t _{D(OFF)}			25		ns
Fall-Time	t _F			18		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				-8	A
Maximum Body-Diode Pulsed Current	I _{SM}				-16	A
Diode Forward Voltage	V _{SD}	I _S =-8.0A, V _{GS} =0V		-0.9	-1.4	V
Body Diode Reverse Recovery Time	t _{rr}	I _S =-8.0A, V _{GS} =0V,		40		ns
Reverse Recovery Charge	Q _{rr}	dl _F /dt=100A/μs (Note 1)		30		ns

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

D.U.T.

V_{DS}

I_{SD}

L

V_{DD}

R_G

V_{GS}

Driver

Same Type as D.U.T.

- * dv/dt controlled by R_G
- * I_{SD} controlled by pulse period
- * D.U.T.-Device Under Test

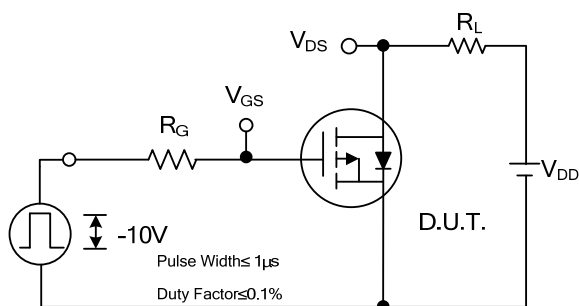
The diagram illustrates the timing relationships for a MOSFET switching event, focusing on the body diode's behavior. The horizontal axis represents time, and the vertical axis represents voltage and current.

- Top Trace (V_{GS} (Driver)):** Shows a square wave pulse. The pulse width is labeled **P.W.**, and the total time for one cycle is labeled **Period**. The duty cycle is given by the formula $D = \frac{P.W.}{Period}$. The peak gate voltage is indicated as $V_{GS} = 10V$.
- Middle Trace (I_{SD} (D.U.T.)):** Shows the source-drain current. During the MOSFET's on-state (when V_{GS} is high), the current is a positive pulse. The peak forward current is labeled I_{FM} , **Body Diode Forward Current**. The slope of this rising edge is labeled di/dt . When the MOSFET turns off, the current reverses, becoming a negative pulse. The peak reverse current is labeled I_{RM} , **Body Diode Reverse Current**.
- Bottom Trace (V_{DS} (D.U.T.)):** Shows the drain-source voltage. During the MOSFET's on-state, V_{DS} is low. When the MOSFET turns off, V_{DS} rises to a level labeled V_{DD} . The initial rise of V_{DS} is labeled **Body Diode Recovery dv/dt** .

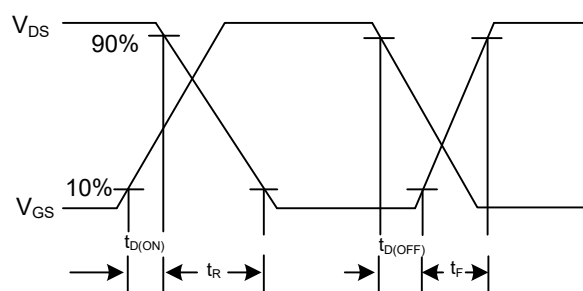
Labels at the bottom of the diagram indicate the regions: **Body Diode** (during the reverse current and recovery phase) and **Forward Voltage Drop** (during the on-state current pulse).

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QW-R210-099.a

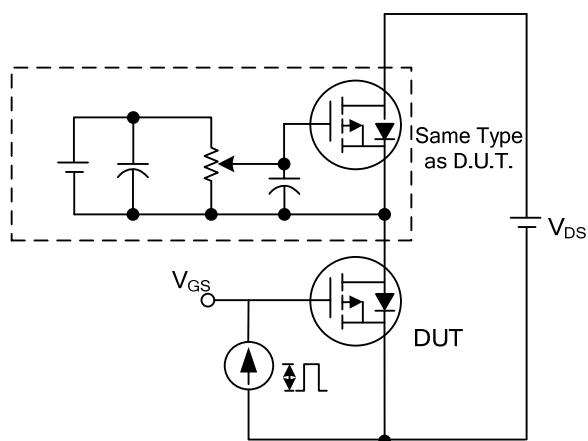
■ TEST CIRCUITS AND WAVEFORMS



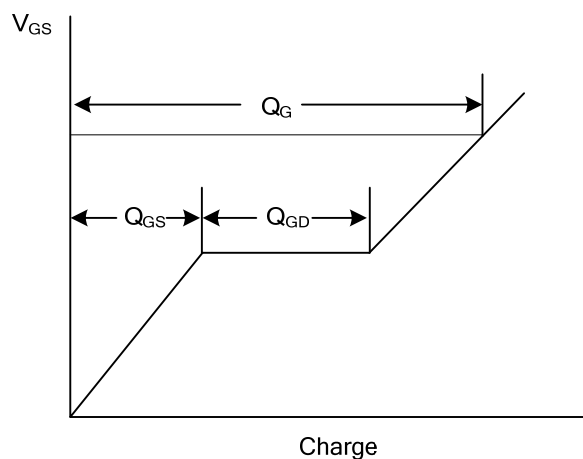
Switching Test Circuit



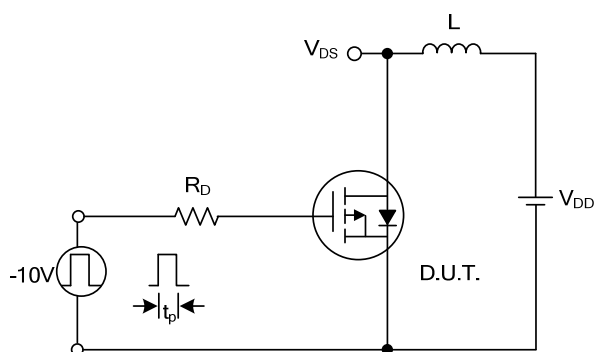
Switching Waveforms



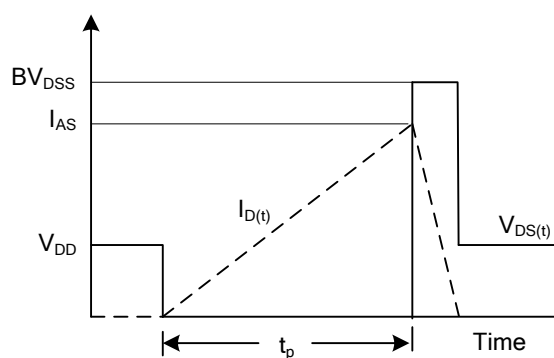
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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