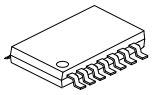
U74GTL2014

CMOS IC

4-CHANNEL LVTTL TO GTL TRANSCEIVER



TSSOP-14

■ DESCRIPTION

The **U74GTL2014** is a 4-channel translator to interface between 3.3-V LV_{TTL} chip set I/O and Xeon processor GTL– / GTL / GTL+ I/O.

■ FEATURES

* Operates as a GTL– / GTL / GTL+ to LV_{TTL} or LV_{TTL} to GTL– / GTL / GTL+ Translator
* The LVTTL Inputs are Tolerant up to 5.5V Allowing Direct Access to TTL or 5V CMOS
* The GTL Input/Output Operate up to 3.6V, Allowing the Device to be Used in High Voltage Open-Drain Applications
* V_{REF} Goes Down to 0.5V for Low Voltage CPU Usage
* Partial Power-Down Permitted

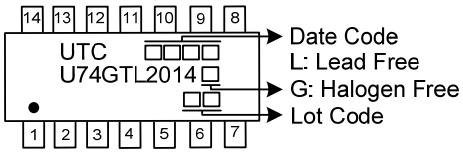
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74GTL2014L-P14-R	U74GTL2014G-P14-R	TSSOP-14	Tape Reel

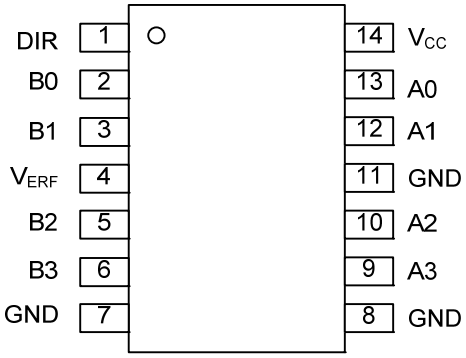
U74GTL2014G-P14-R
- (1)Packing Type
- (2)Package Type
- (3)Green Package

(1) R: Tape Reel
(2) P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



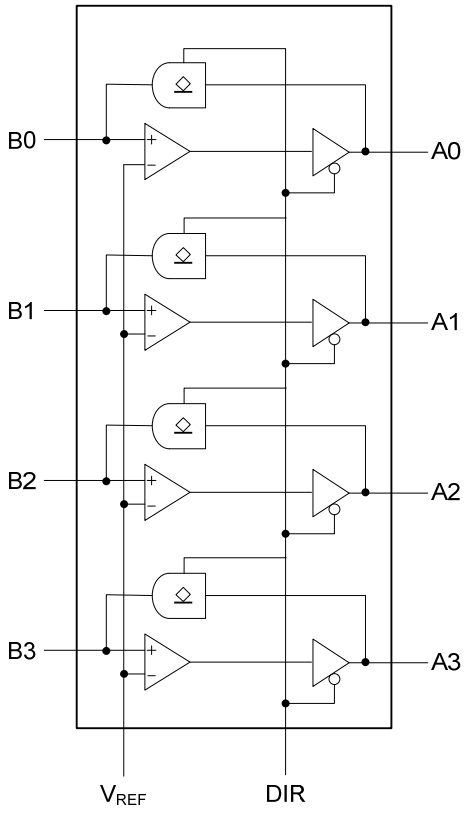
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	DIR	Direction control input (LVTTL)
2	B0	GTL data input/output
3	B1	
5	B2	
6	B3	
7, 8, 11	GND	Ground
9	A3	LVTTL data input/output
10	A2	
12	A1	
13	A0	
14	V_{CC}	Supply voltage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=-40~+85°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 4.6	V
Input Voltage	V_{IN}	A port	-0.5 ~ 7.0	V
		B port	-0.5 ~ 4.6	V
Output Voltage	V_{OUT}	A port	-0.5 ~ 7.0	V
		B port	-0.5 ~ 4.6	V
Input Control Voltages SEL (Note 2)	V_{SEL}		-0.5 ~ 6.0	V
Input Clamp Current	I_{IK}	V_{IN} < 0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT} < 0V	-50	mA
Current Into Any Output In The Low State	I_{OL}	A port	40	mA
		B port	80	mA
Current Into Any Output In The High State	I_{OH}		-40	mA
Junction Temperature	T_J		+150	°C
Storage Temperature Range	T_{STG}		-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. V_I and V_O are used to denote specific conditions for $V_{I/O}$.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	3.0	3.3	3.6	V
Input Voltage	A port	V_{IN}	0	3.3	5.5 (Note 2)	V
	B port		0	V_{TT}	3.6	V
Termination Voltage	GTL-	V_{TT}	0.85	0.9	0.95	V
	GTL		1.14	1.2	1.26	V
	GTL+		1.35	1.5	1.65	V
Reference Voltage	Overall	V_{REF}	0.5	2 / 3 V_{TT}	V_{CC} / 2	V
	GTL-		0.5	0.6	0.63	V
	GTL		0.76	0.8	0.84	V
	GTL+		0.87	1.0	1.1	V
Operating Temperature		T_A	-40		+85	°C

Notes: 1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
2. The $V_{I(Max.)}$ of LV_{TTL} port is 3.6V if configured as output (DIR=L).

■ ELECTRICAL CHARACTERISTICS (T_A=-40°C~+85°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	A port	V_{IH}		2			V
	B port			V_{REF}+ 50mV			V
Low-Lever Output Voltage	A port	V_{IL}				0.8	V
	B port					V_{REF}- 50mV	V
High-Level Input Current	A port	I_{OH}				-20	mA
Low-Level Input Current	A port	I_{OL}				20	mA
	B port					50	mA
High-Level Output Voltage	A port	V_{OH}	V_{CC}=3~3.6V, I_{OH}=-100μA	V_{CC} -0.2			V
			V_{CC}=3V, I_{OH}=-16mA	2			V
Low-Level Output Voltage	A port	V_{OL}	V_{CC}=3V, I_{OH}=8mA		0.28	0.4	V
			V_{CC}=3V, I_{OH}=16mA		0.55	0.8	V
	B port		V_{CC}=3V, I_{OH}=40mA		0.23	0.4	V
Input Leakage Current	A port	$I_{I(LEAK)}$	V_{CC}=3.6V, V_{IN}=V_{CC}			±1	μA
			V_{CC}=3.6V, V_{IN}=0V			±1	μA
			V_{CC}=3.6V, V_{IN}=5.5V			5	μA
	B port		V_{CC}=3.6V, V_{IN}=V_{TT} or GND			±1	μA
	Control Pin		V_{CC}=3.6V, V_{IN}=V_{CC} or 0V			±1	μA
OFF-state output current	A port	I_{OFF}	V_{CC}=0V, V_{IO}=0~3.6V			±10	μA
			V_{CC}=0V, V_{IO}=3.6~5.5V			±100	μA
	B port		V_{CC}=0V, V_{IO}=0~3.6V			±10	μA
Quiescent Supply Current	A port	I_{CC}	V_{CC}=3.6V, V_{IN}=V_{CC} or GND, I_{OUT}=0		3	10	mA
	B port		V_{CC}=3.6V, V_{IN}=V_{TT} or GND, I_{OUT}=0		3	10	mA
Additional Quiescent Supply Current Per Input Pin		ΔI_{CC}	V_{CC}=3.6V, V_{IN}= V_{CC}-0.6V			500	μA

■ DYNAMIC CHARACTERISTICS

(V_{CC}=1.65 to 4.6V, GND=0V for GTL T_A=-40~+85°C, T_A=-40°C~+85°C, unless otherwise specified)

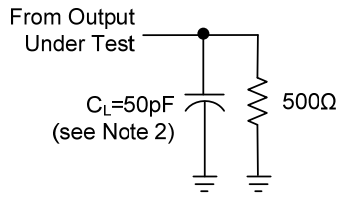
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low to High Propagation Delay From Input (An) to Output (Bn)	GTL-	t_{PLH}	V_{CC}=3.3V±0.3V V_{REF}=0.6V, V_{TT}=0.9V		5	7	ns
	GTL		V_{CC}=3.3V±0.3V V_{REF}=0.8V, V_{TT}=1.2V		5	7	ns
	GTL+		V_{CC}=3.3V±0.3V V_{REF}=1.0V, V_{TT}=1.5V		5	7	ns
High to Low Propagation Delay From Input (An) to Output (Bn)	GTL-	t_{PHL}	V_{CC}=3.3V±0.3V V_{REF}=0.6V, V_{TT}=0.9V		5.9	7.9	ns
	GTL		V_{CC}=3.3V±0.3V V_{REF}=0.8V, V_{TT}=1.2V		6	8	ns
	GTL+		V_{CC}=3.3V±0.3V V_{REF}=1.0V, V_{TT}=1.5V		6	8	ns
Low to High Propagation Delay From Input (Bn) to Output (An)	GTL-	t_{PLH}	V_{CC}=3.3V±0.3V V_{REF}=0.6V, V_{TT}=0.9V		8.3	10	ns
	GTL		V_{CC}=3.3V±0.3V V_{REF}=0.8V, V_{TT}=1.2V		8.2	10	ns
	GTL+		V_{CC}=3.3V±0.3V V_{REF}=1.0V, V_{TT}=1.5V		8.1	10	ns
High to Low Propagation Delay From Input (Bn) to Output (An)	GTL-	t_{PHL}	V_{CC}=3.3V±0.3V V_{REF}=0.6V, V_{TT}=0.9V		9.2	11	ns
	GTL		V_{CC}=3.3V±0.3V V_{REF}=0.8V, V_{TT}=1.2V		8.9	10.5	ns
	GTL+		V_{CC}=3.3V±0.3V V_{REF}=1.0V, V_{TT}=1.5V		8.7	10.5	ns

■ OPERATING CHARACTERISTIC

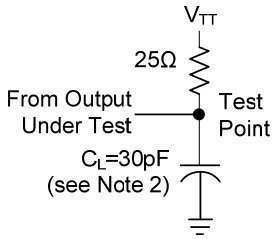
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance		C_{IN}	V_{IN}=3V or 0V		2.5	3.0	pF
Output Capacitance	A port	C_{IO}	V_{OUT}=3V or 0V		7.5	9.5	pF
	B port		V_{OUT}=V_{TT} or 0V		5.5	6.0	pF

■ TEST CIRCUIT AND WAVEFORMS

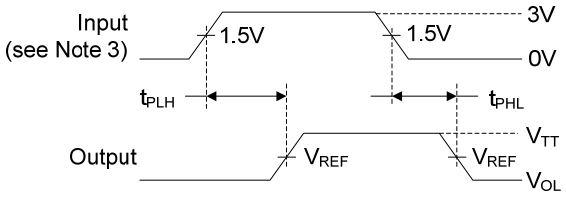
(V_{TT}=1.2V, V_{REF}=0.8V for GTL and V_{TT}=1.5V, V_{REF}=1V For GTL+.)



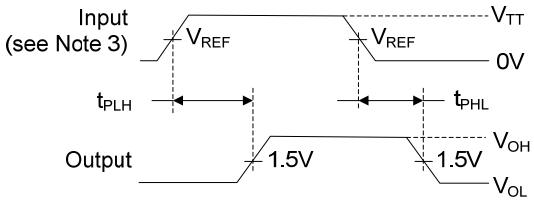
LOAD CIRCUIT FOR A OUTPUTS



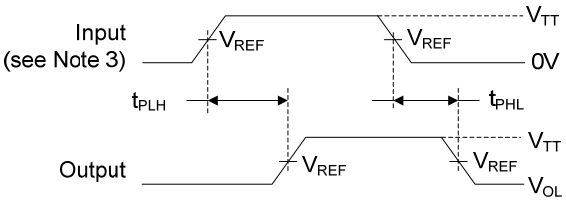
LOAD CIRCUIT FOR B OUTPUTS



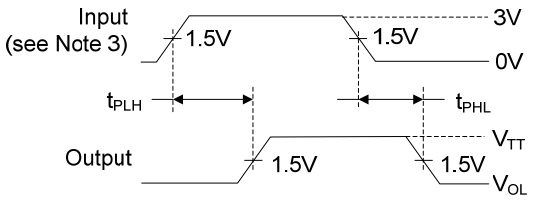
VOLTAGE WAVEFORM 1
PROPAGATION DELAY TIMES
(A Port to B Port) (NOTE 1)



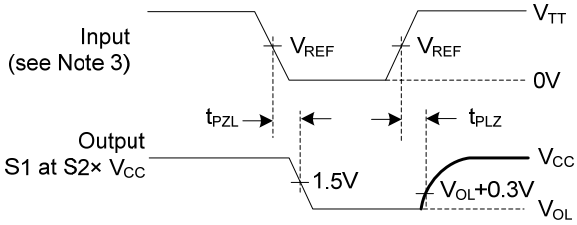
VOLTAGE WAVEFORM 2
PROPAGATION DELAY TIMES
(B Port to A Port) (NOTE 1)



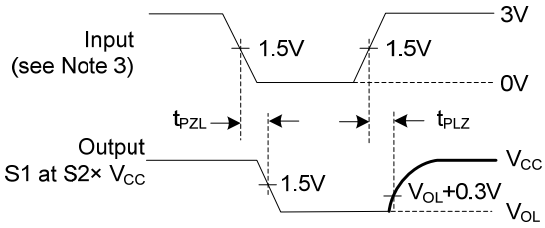
VOLTAGE WAVEFORM 3
PROPAGATION DELAY TIMES
(B Port to B Port) (NOTE 1)



VOLTAGE WAVEFORM 4
PROPAGATION DELAY TIMES
(ENn to A Port) (NOTE 1)



VOLTAGE WAVEFORM 5
PROPAGATION DELAY TIMES
(B Port to A (I/O) Port) (NOTE 1)



VOLTAGE WAVEFORM 6
ENABLE AND DISABLETIMES
(EN2 to A (I/O) Port) (NOTE 1)

Notes: 1. All control inputs are LV_{TTL} levels.
2. C_L includes probe and jig capacitance.
3. All input pulses are supplied by generators having the following characteristics: $P_{RR} \le$ 10MHz, Z_O=50Ω, $t_r \le$ 2.5ns, $t_r \le$ 2.5ns.
4. The outputs are measured one at a time, with one transition per measurement.

■ APPLICATION AND IMPLEMENTATION

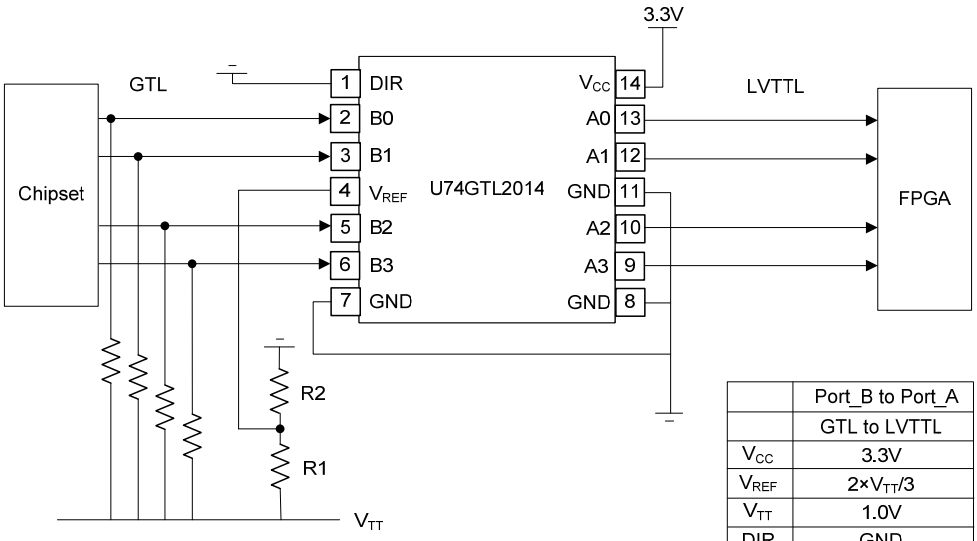
Application Information

U74GTL2014 is the voltage translator for GTL– /GTL / GTL+ to LV_{TTL} or LV_{TTL} to GTL– / GTL / GTL+. Please find the reference schematic and recommend value for passive component in the Typical Application.

■ TYPICAL APPLICATION

1. GTL– /GTL / GTL+ to LV_{TTL}:

Select appropriate V_{TT} / V_{REF} based upon GTL– / GTL / GTL+. The parameters in Recommended Operating Conditions are compliant to the GTL specification.



	Port_B to Port_A
	GTL to LVTTL
V_{CC}	3.3V
V_{REF}	$2\times V_{TT}/3$
V_{TT}	1.0V
DIR	GND
R	75Ω
R1	49.9Ω
R2	100Ω

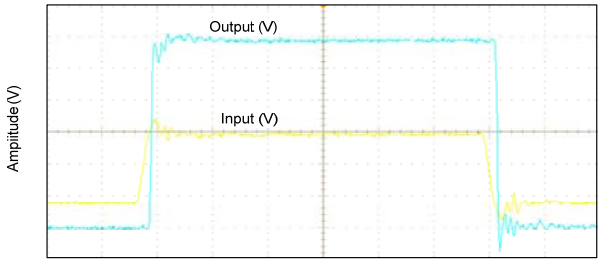
Application Diagram for GTL to LV_{TTL}

1.1 Detailed Design Procedure

To begin the design process, determine the following:

1. Select direction base upon application (GTL– / GTL / GTL+ to LV_{TTL} or LV_{TTL} to GTL– / GTL / GTL+).
2. Set up appropriate DIR pin and V_{REF} / V_{TT}.
3. Choose correct pullup resistor value base upon data rate and driving current requirement (for LV_{TTL} to GTL– / GTL / GTL+).

1.2 Application Curve

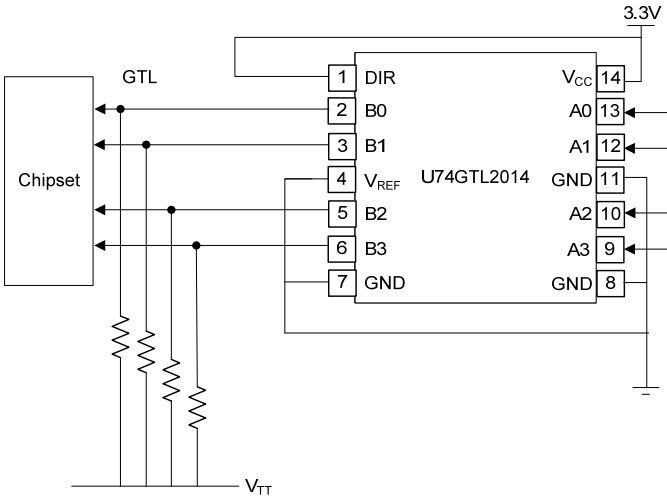


GTL-to-LV_{TTL}, V_{REF}=1V, V_{IN}=1.5V, 100MHz

■ TYPICAL APPLICATION (Cont.)

2. LV_{TTL}/TTL to GTL– /GTL / GTL+:

Because GTL is an open-drain interface, the selection of pullup resistor depends on the application requirement (for example, data rate) and PCB trace capacitance.



	Port_A to Port_B
	LVTTL to GTL
V_{CC}	3.3V
V_{REF}	GND
V_{TT}	1.0V
DIR	3.3V
R	75Ω
R1	Not Avaliable
R2	Not Avaliable

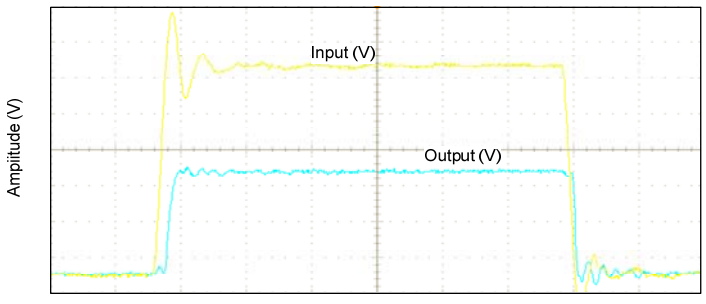
Application Diagram for LV_{TTL} to GTL

2.1 Detailed Design Procedure

To begin the design process, determine the following:

1. Select direction based upon application (GTL– / GTL / GTL+ to LV_{TTL} or LV_{TTL} to GTL– / GTL / GTL+).
2. Set up appropriate DIR pin and V_{REF} / V_{TT}.
3. Choose correct pullup resistor value base upon data rate and driving current requirement (for LV_{TTL} to GTL– / GTL / GTL+).

2.2 Application Curve



LV_{TTL}-to-GTL, V_{REF}=1V, V_{TT}=1.5V, 10MHz

■ TYPICAL CHARACTERISTICS