

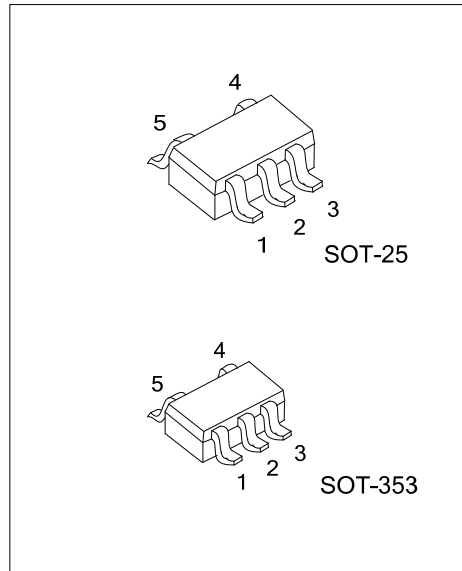


## U74LV1T125

Preliminary

CMOS IC

### SINGLE POWER SUPPLY SINGLE BUFFER GATE WITH 3-STATE OUTPUT CMOS LOGIC LEVEL SHIFTER



#### DESCRIPTION

The **U74LV1T125** is a single, level translating buffer driver with 3-state output. The 3-state output is controlled by the output enable input (OE). A HIGH-level at OE causes the output to assume a high-impedance OFF-state. The output level is referenced to the supply voltage and supports 1.8V, 2.5V, 3.3V and 5.0V CMOS levels. The low threshold inputs support 1.8V input logic at  $V_{CC} = 3.3V$  and can be used in 1.8V to 3.3V level up translation. In addition, the 5V tolerant input pins enable down translation (3.3V to 2.5V output at  $V_{CC} = 2.5V$ ). The wide  $V_{CC}$  range permits the generation of output levels to connect to controllers or processors.

#### FEATURES

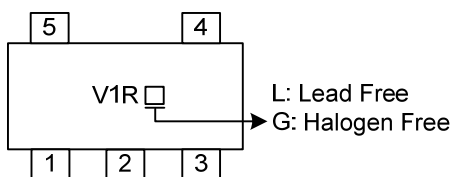
- \* Single supply voltage translator at 1.8V, 2.5V, 3.3V and 5.0V
- \* Low Power Current 10 $\mu$ A (Max.)
- \*  $\pm 8mA$  Output Drive ( $V_{CC}=5.0V$ )

#### ORDERING INFORMATION

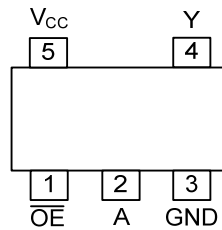
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LV1T125L-AF5-R	U74LV1T125G-AF5-R	SOT-25	Tape Reel
U74LV1T125L-AL5-R	U74LV1T125G-AL5-R	SOT-353	Tape Reel

<p>U74LV1T125G-AF5-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) AF5: SOT-25, AL5: SOT-353</p> <p>(3) G: Halogen Free and Lead Free, K: Lead Free</p>
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#### MARKING



### ■ PIN CONFIGURATION



### ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{OE}$	Output enable, active low
2	A	Input A
3	GND	Ground
4	Y	Output Y
5	V <sub>CC</sub>	Positive supply

Note: I=Input, O=Output, I/O= Input or Output, G=Ground, P=Power

### ■ FUNCTION TABLE (each gate)

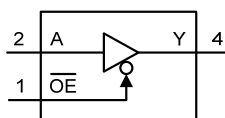
INPUT (Lower Level Input)		OUTPUT (V <sub>CC</sub> CMOS)
$\overline{OE}$ (Note 3)	A	Y
L	H	H
L	L	L
H	X	Z

Notes: 1. H = HIGH Voltage Level; L = LOW Voltage Level; X = Do don't care; Z = high-impedance.

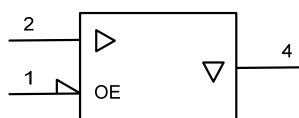
2. H = Driving High; L = Driving Low; Z = High-Impedance State.

3. Not recommend to float  $\overline{OE}$  pin for signal oscillation.

### ■ LOGIC DIAGRAM (positive logic)

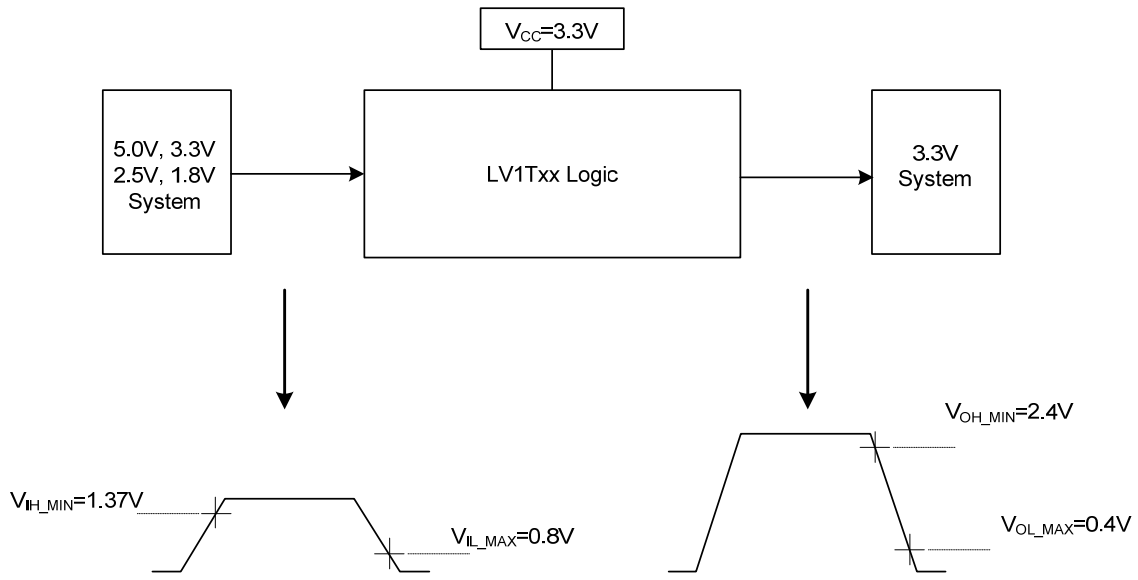
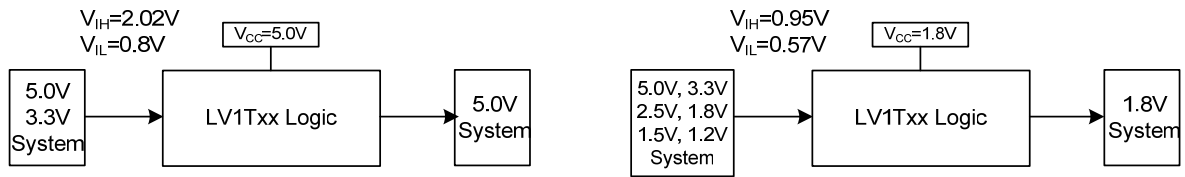


Logic Symbol



IEC Logic Symbol

■ TYPICAL DESIGN EXAMPLES



Switching Thresholds for 1.8V~3.3V Translation

ABSOLUTE MAXIMUM RATING ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified) (Note 2)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	$V_{CC}$		-0.5 ~ 7	V
Input Voltage (Note 2)	$V_{IN}$		-0.5 ~ 7	V
Output Voltage (Note 2)	$V_{OUT}$	Output HIGH or LOW state	-0.5 ~ $V_{CC}+0.5$	V
		Output in power-off state	-0.5 ~ 4.6	V
Continuous Output Current	$I_{OUT}$		$\pm 25$	mA
Continuous current through		$V_{CC}$ or GND	$\pm 50$	mA
Input Clamp Current	$I_{IK}$	$V_{IN} < 0$	-20	mA
Output Clamp Current	$I_{OK}$	$V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	$\pm 20$	mA
Storage Temperature Range	$T_{STG}$		-65 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

#### ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	Operating	1.6		5.5	V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=1.8\text{V}$			20	ns/V
		$V_{CC}=3.3\text{V}$ or $2.5\text{V}$			20	ns/V
		$V_{CC}=5\text{V}$			20	ns/V
Operating Temperature	$T_A$		-40		+125	$^{\circ}\text{C}$

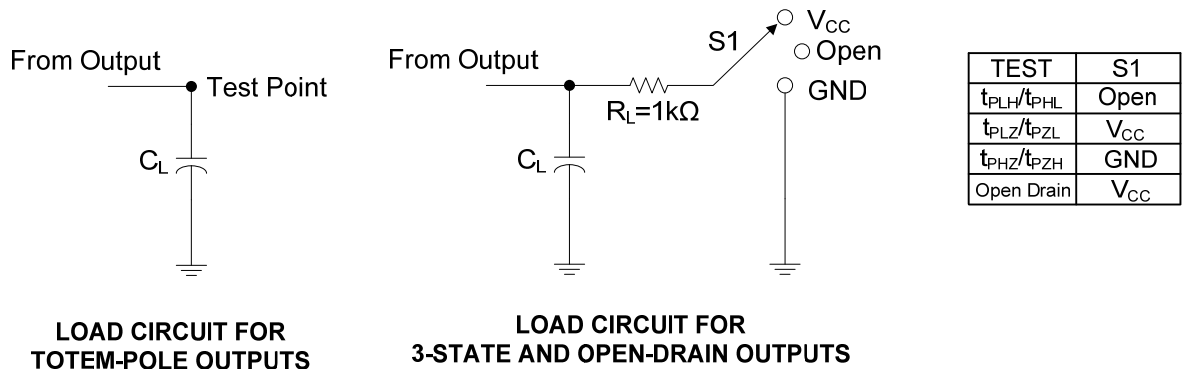
■ STATIC CHARACTERISTICS (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-Level Input Voltage	V <sub>IH</sub>	V <sub>CC</sub> =1.65V~1.8V	0.95			V	
		V <sub>CC</sub> =2.0V	0.99			V	
		V <sub>CC</sub> =2.25V~2.5V	1.145			V	
		V <sub>CC</sub> =2.75V	1.22			V	
		V <sub>CC</sub> =3V~3.3V	1.37			V	
		V <sub>CC</sub> =3.6V	1.47			V	
		V <sub>CC</sub> =4.5V~5.0V	2.02			V	
		V <sub>CC</sub> =5.5V	2.1			V	
Low-Level Input Voltage	V <sub>IL</sub>	V <sub>CC</sub> =1.65V~2V			0.57	V	
		V <sub>CC</sub> =2.25V~2.75V			0.75	V	
		V <sub>CC</sub> =3V~3.6V			0.8	V	
		V <sub>CC</sub> =4.5V~5.5V			0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>CC</sub> =1.65V ~ 5.5V, I <sub>OH</sub> =-20μA	V <sub>CC</sub> -0.1			V	
		V <sub>CC</sub> =1.65V	I <sub>OH</sub> =-2mA	1.28		V	
		V <sub>CC</sub> =1.8V		1.5		V	
		V <sub>CC</sub> =2.3V, I <sub>OH</sub> =-3mA	2		V		
		V <sub>CC</sub> =2.5V, I <sub>OH</sub> =-3mA	2.25		V		
		V <sub>CC</sub> =3V	I <sub>OH</sub> =-3mA I <sub>OH</sub> =-5.5mA	2.78		V	
		V <sub>CC</sub> =3.3V, I <sub>OH</sub> =-5.5mA		2.9		V	
		V <sub>CC</sub> =4.5V	I <sub>OH</sub> =-4mA I <sub>OH</sub> =-8mA	4.2		V	
		V <sub>CC</sub> =5V, I <sub>OH</sub> =-8mA		4.6		V	
		Low-Level Output Voltage	V <sub>OL</sub>	V <sub>CC</sub> =1.65V ~ 5.5V, I <sub>OL</sub> =20μA			0.1
V <sub>CC</sub> =1.65V, I <sub>OL</sub> =2mA					0.2	V	
V <sub>CC</sub> =2.3V, I <sub>OL</sub> =3mA					0.15	V	
V <sub>CC</sub> =3V	I <sub>OL</sub> =3mA I <sub>OL</sub> =5.5mA					0.11	V
V <sub>CC</sub> =4.5V				I <sub>OL</sub> =4mA I <sub>OL</sub> =8mA			0.15
							0.3
A Input Leakage Current	I <sub>I(LEAK)</sub>	A Input V <sub>CC</sub> =0V, 1.8V, 2.5V, 3.3V, 5.5V, V <sub>IN</sub> =0V or V <sub>CC</sub>			0.1	μA	
Quiescent Supply Current	I <sub>Q</sub>	V <sub>CC</sub> =1.8V, 2.5V, 3.3V, 5V, V <sub>IN</sub> =0V or V <sub>CC</sub> , I <sub>O</sub> =0; Open on loading			1	μA	
Additional Quiescent Supply Current	ΔI <sub>Q</sub>	V <sub>CC</sub> =5.5V, one input at 0.3V or 3.4V, other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> =0			1.35	mA	
		V <sub>CC</sub> =1.8V, one input at 0.3V or 1.1V, other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> =0			10	μA	
Input Capacitance	C <sub>IN</sub>	V <sub>CC</sub> =3.3V, V <sub>IN</sub> =V <sub>CC</sub> or GND		2		pF	
Output Capacitance	C <sub>OUT</sub>	V <sub>CC</sub> =3.3V, V <sub>OUT</sub> =V <sub>CC</sub> or GND		2.5		pF	
Power Dissipation Capacitance	C <sub>PD</sub>	f=1MHz and 10MHz	V <sub>CC</sub> =1.8V±0.15V		14		pF
			V <sub>CC</sub> =2.5V±0.2V		14		pF
			V <sub>CC</sub> =3.3V±0.3V		14		pF
			V <sub>CC</sub> =5V±0.5V		14		pF

■ DYNAMIC CHARACTERISTICS (T<sub>A</sub>=25°C, unless otherwise specified)

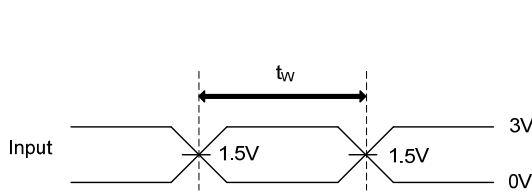
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Propagation delay from input (Any In) to output(Y)	t <sub>PLH</sub> /t <sub>PHL</sub>	C <sub>L</sub> =15pF	V <sub>CC</sub> =1.8V		10.5	13	ns
			V <sub>CC</sub> =2.5V		5.8	8.5	ns
			V <sub>CC</sub> =3.3V		4.0	7.0	ns
			V <sub>CC</sub> =5V		2.7	5.5	ns
		C <sub>L</sub> =30pF	V <sub>CC</sub> =1.8V		12	14.5	ns
			V <sub>CC</sub> =2.5V		6.5	9.5	ns
			V <sub>CC</sub> =3.3V		4.9	8.0	ns
			V <sub>CC</sub> =5V		3.0	6.5	ns
Propagation delay from input ( $\overline{OE}$ ) to output(Y)	t <sub>PZH</sub> /t <sub>PZL</sub>	C <sub>L</sub> =15pF	V <sub>CC</sub> =1.8V		9.0	12	ns
			V <sub>CC</sub> =2.5V		5.5	8.0	ns
			V <sub>CC</sub> =3.3V		4.0	6.5	ns
			V <sub>CC</sub> =5V		3.0	5.0	ns
		C <sub>L</sub> =30pF	V <sub>CC</sub> =1.8V		12.5	15	ns
			V <sub>CC</sub> =2.5V		7.0	10	ns
			V <sub>CC</sub> =3.3V		5.0	8.0	ns
			V <sub>CC</sub> =5V		4.3	6.5	ns
Propagation delay from input ( $\overline{OE}$ ) to output(Y)	t <sub>PHZ</sub> /t <sub>PLZ</sub>	C <sub>L</sub> =15pF	V <sub>CC</sub> =1.8V		8.0	10	ns
			V <sub>CC</sub> =2.5V		5.0	11	ns
			V <sub>CC</sub> =3.3V		4.5	7.0	ns
			V <sub>CC</sub> =5V		4.2	6.5	ns
		C <sub>L</sub> =30pF	V <sub>CC</sub> =1.8V		8.5	11	ns
			V <sub>CC</sub> =2.5V		6.0	9.0	ns
			V <sub>CC</sub> =3.3V		5.0	8.0	ns
			V <sub>CC</sub> =5V		4.8	8.0	ns

### TEST CIRCUIT AND WAVEFORMS

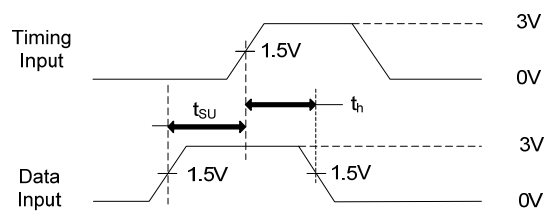


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

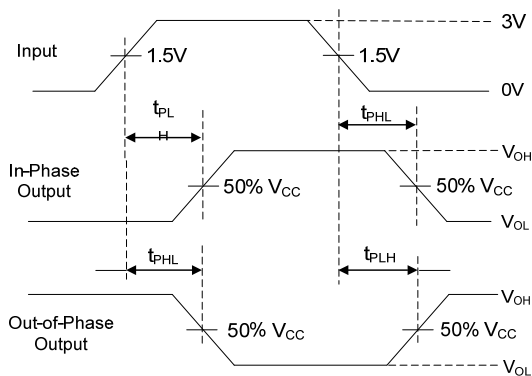
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



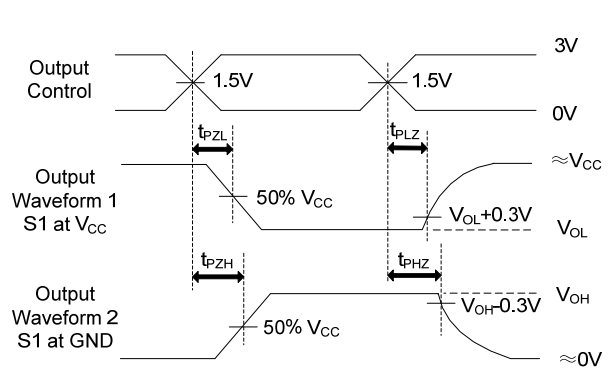
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

- Notes: 1. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1MHz,  $Z_0=50\Omega$ ,  $t_r \leq 3ns$ .  
 2. The outputs are measured one at a time, with one transition per measurement.

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