

**UT25P012L**

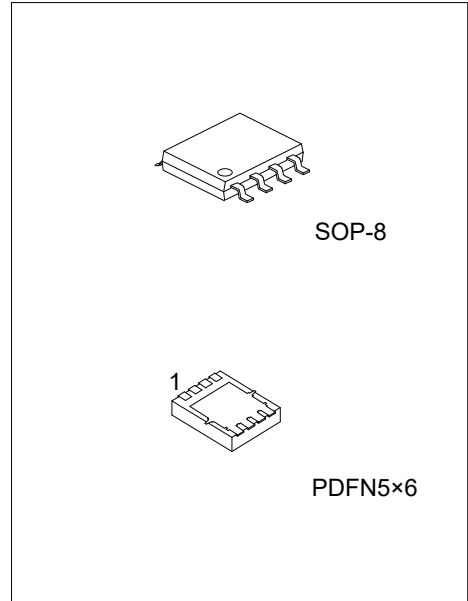
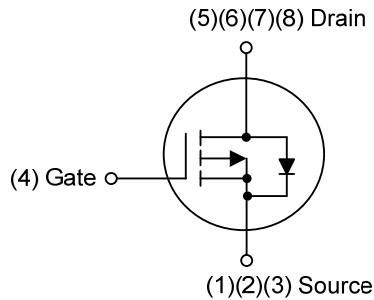
Preliminary

POWER MOSFET**-25A, -12V P-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT25P012L** is a P-channel MOS Field Effect Transistor. it uses UTC's advanced technology to provide the customers with high switching speed and a minimum on-state resistance.

FEATURES

- * $R_{DS(ON)} \leq 5.0 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -16\text{A}$
- $R_{DS(ON)} \leq 7.0 \text{ m}\Omega$ @ $V_{GS} = -2.5\text{V}$, $I_D = -13.6\text{A}$

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT25P012LK-S08-R	UT25P012LG-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT25P012LK-P5060-R	UT25P012LG-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

UT25P012LG-S08-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) S08: SOP-8, P5060: PDFN5x6
		(3) Green Package	(3) G: Halogen Free and Lead Free, K: Lead Free

MARKING

SOP-8	PDFN5x6
8 7 6 5 UTC □ □ □ □ UT25P012L □ • □ □ 1 2 3 4 → Date Code K: Lead Free G: Halogen Free → Lot Code	UTC UT 25P012L • □ □ □ □ □ □ ← Lot Code → Date Code

■ **ABSOLUTE MAXIMUM RATING** ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-12	V
Gate-Source Voltage		V_{GSS}	± 8	V
Drain Current	DC	I_D	-25	A
	Pulsed (Note 2)	I_{DM}	-50	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	338	mJ
Power Dissipation	SOP-8	P_D	7	W
	PDFN5×6		62	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 1\text{mH}$, $I_{AS} = -26\text{A}$, $V_{DD} = -50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	125	$^{\circ}\text{C/W}$
	PDFN5×6		65	$^{\circ}\text{C/W}$
Junction to Case	SOP-8	θ_{JC}	7	$^{\circ}\text{C/W}$
	PDFN5×6		2	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

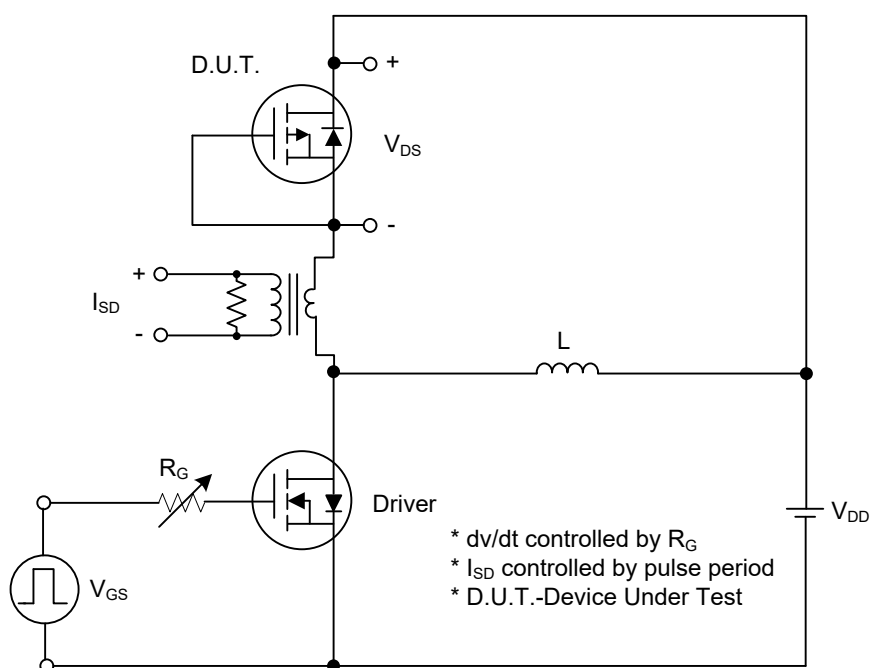
■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =-250μA	-12			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-12V, V _{GS} =0V			-1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+8V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-8V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D =-250μA	-0.3		-1.2	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =-4.5V, I _D =-16A			5.0	mΩ
			V _{GS} =-2.5V, I _D =-13.6A			7.0	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-10V, f=1.0MHz		11		nF
Output Capacitance		C _{OSS}			3.3		nF
Reverse Transfer Capacitance		C _{RSS}			2.5		nF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =-9.6V, V _{GS} =-10V, I _D =-25A (Note 1, 2)		231		nC
Gate to Source Charge		Q _{GS}			9		nC
Gate to Drain Charge		Q _{GD}			8		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DS} =-6V, V _{GS} =-10V, I _D =-25A, R _G =3Ω (Note 1, 2)		15		ns
Rise Time		t _R			19		ns
Turn-OFF Delay Time		t _{D(OFF)}			529		ns
Fall-Time		t _F			421		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				-25	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				-50	A
Diode Forward Voltage		V _{SD}	I _F =-25A, V _{GS} =0V			-1.4	V

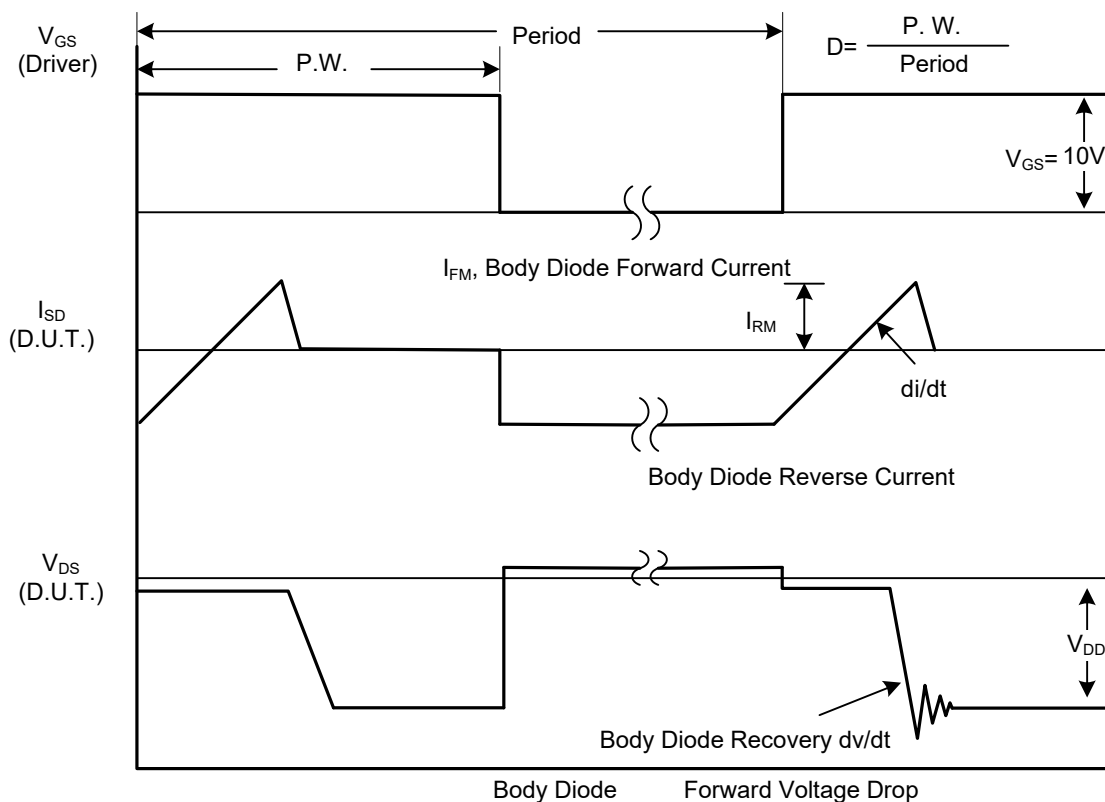
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

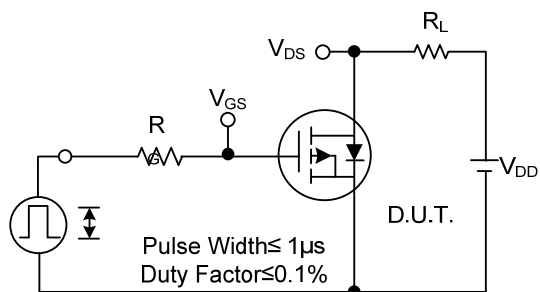


Peak Diode Recovery dv/dt Test Circuit

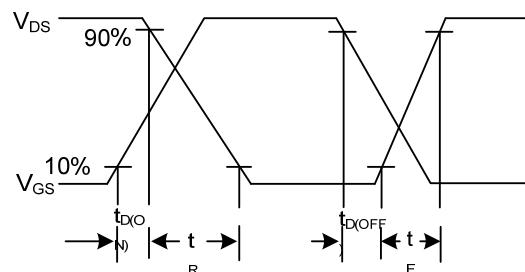


Peak Diode Recovery dv/dt Waveforms

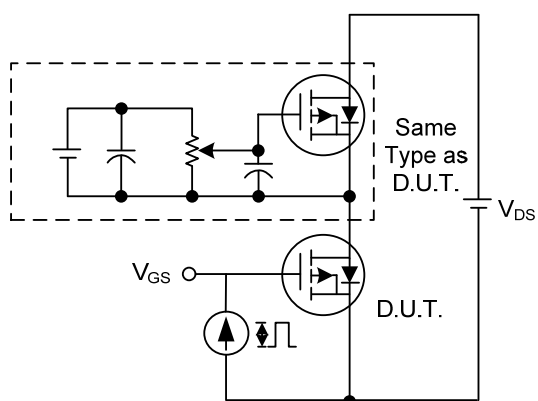
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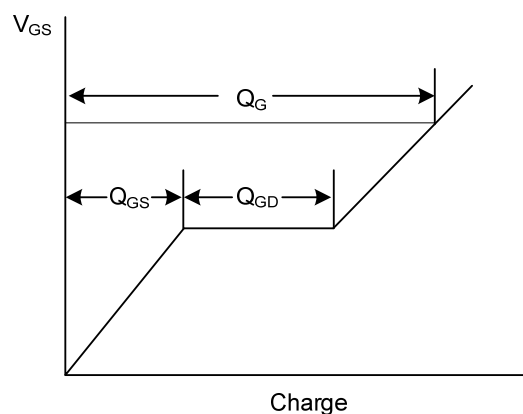
Switching Test Circuit



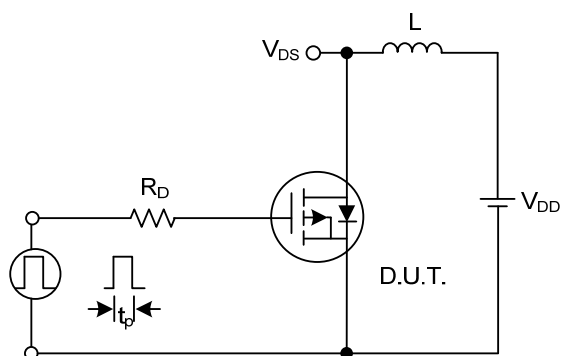
Switching Waveforms



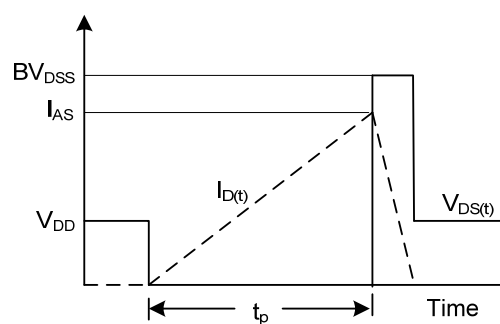
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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