



UT30P10

Preliminary

Power MOSFET

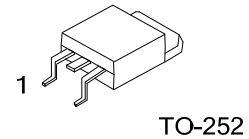
-30A, -100V P-CHANNEL POWER MOSFET

DESCRIPTION

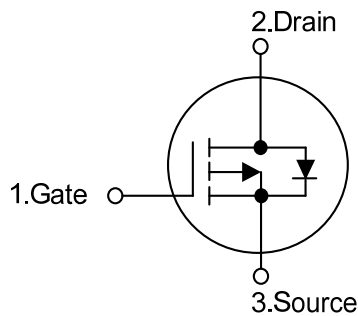
The UTC **UT30P10** provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

FEATURES

- * $R_{DS(ON)} \leq 65 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -15\text{A}$
 $R_{DS(ON)} \leq 80 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -10\text{A}$
- * High Switching Speed
- * 100% Avalanche Tested



SYMBOL



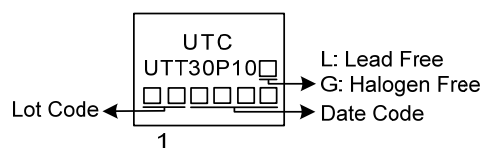
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT30P10L-TN3-R	UT30P10G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT30P10G-TN3-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>		<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	-100	V
Gate-Source Voltage			V_{GSS}	± 20	V
Drain Current	Continuous, $T_C=25^\circ\text{C}$		I_D	-30	A
	Pulsed (Note 2)		I_{DM}	-60	A
Avalanche Energy	Repetitive (Note 3)		E_{AS}	73	mJ
Peak Diode Recovery dv/dt (Note 4)			dv/dt	3.9	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)			P_D	50	W
Junction Temperature			T_J	+150	$^\circ\text{C}$
Storage Temperature			T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = -38.2\text{A}$, $V_{DD} = -50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq -30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case		θ_{JC}	2.5 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

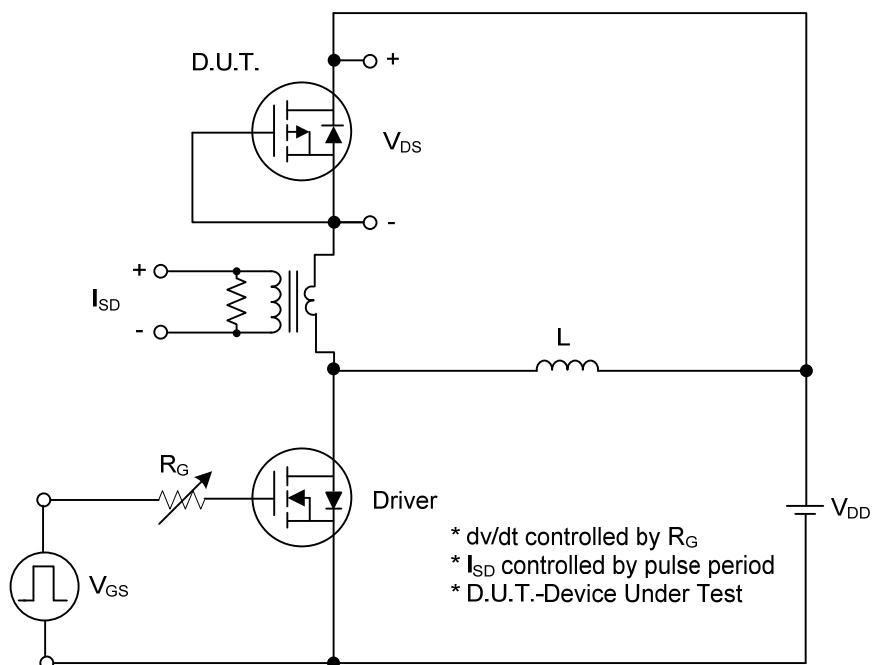
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =-250μA, V _{GS} =0V	-100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-100V, V _{GS} =0V			-1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-2.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =-10V, I _D =-15A			65	mΩ
			V _{GS} =-4.5V, I _D =-10A			80	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =-25V, V _{GS} =0V, f=1MHz		3186		pF
Output Capacitance		C _{OSS}			157		pF
Reverse Transfer Capacitance		C _{RSS}			123		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =-80V, V _{GS} =-10V, I _D =-30A (Note 1, 2)		52		nC
Gate to Source Charge		Q _{GS}			8		nC
Gate to Drain Charge		Q _{GD}			18		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DS} =-50V, I _D =-30A, R _G =3Ω (Note 1, 2)		12		ns
Rise Time		t _R			16		ns
Turn-OFF Delay Time		t _{D(OFF)}			50		ns
Fall-Time		t _F			23		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				-30	A
Maximum Body-Diode Pulsed Current		I _{SM}	(Note 1)			-60	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =-30A, V _{GS} =0V (Note 2)			-1.4	V
Body Diode Reverse Recovery Time (Note 1)		t _{rr}	I _S =-30A, V _{GS} =0V,		127		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		203		nC

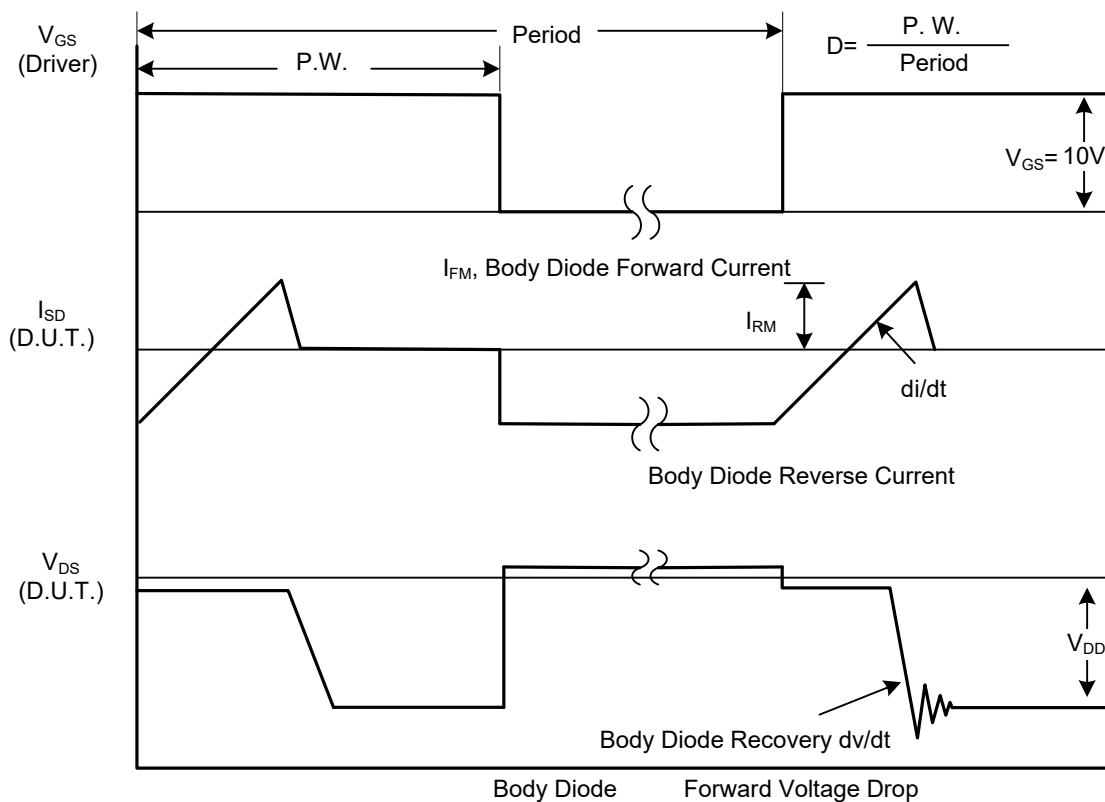
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

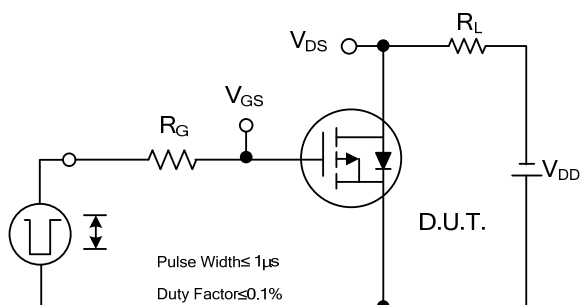


Peak Diode Recovery dv/dt Test Circuit

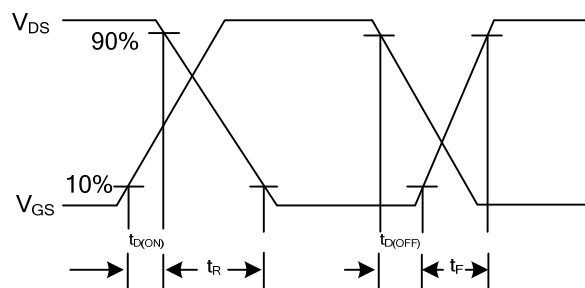


Peak Diode Recovery dv/dt Waveforms

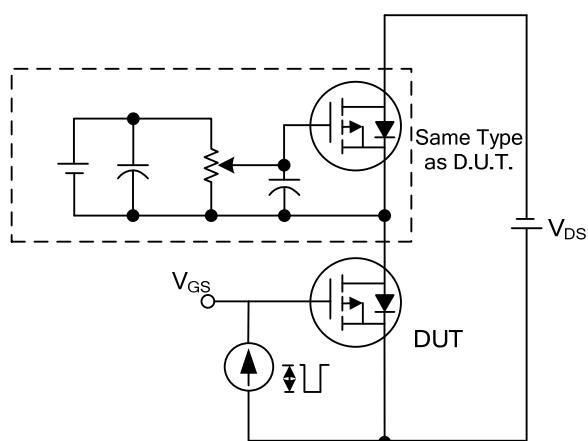
■ TEST CIRCUITS AND WAVEFORMS



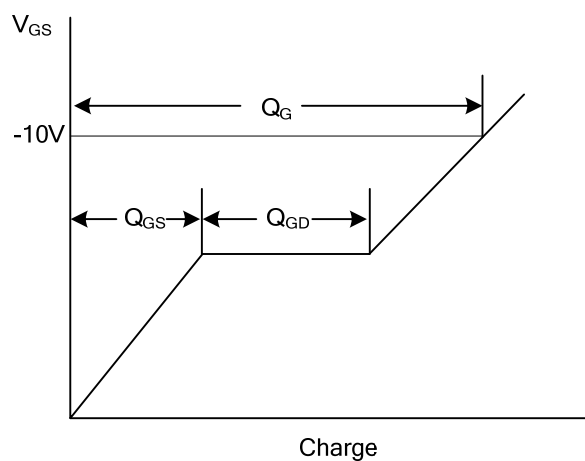
Switching Test Circuit



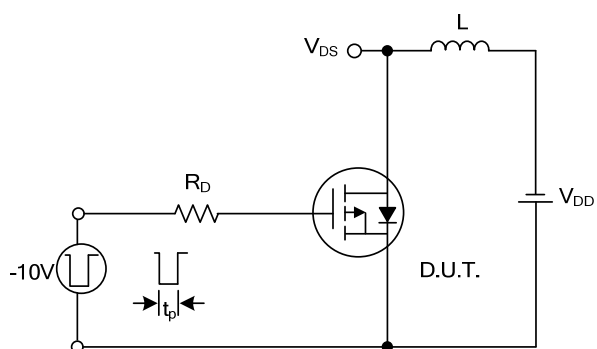
Switching Waveforms



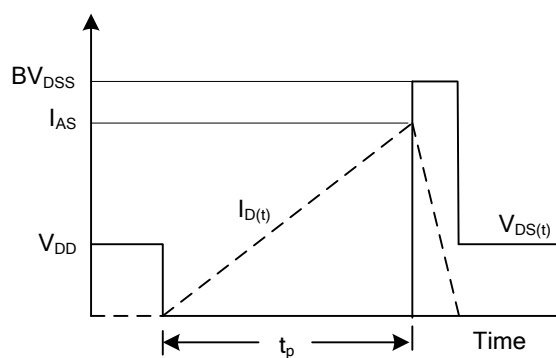
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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