



UT40N04HZ

Preliminary

Power MOSFET

40A, 40V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

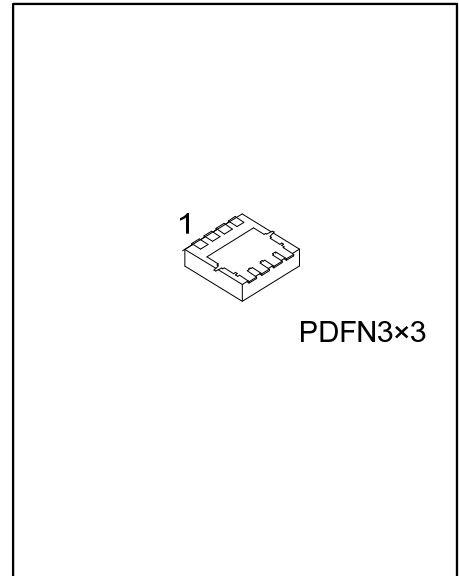
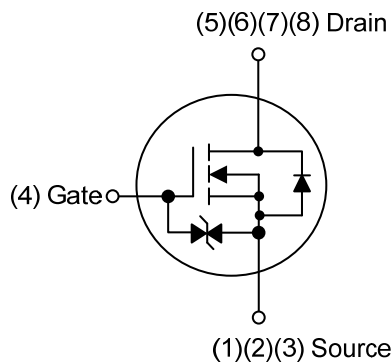
DESCRIPTION

The UTC **UT40N04HZ** is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

FEATURES

- * $R_{DS(ON)} \leq 10 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
- * Low drain-source on-resistance
- * Low leakage current?
- * Enhancement mode
- * With ESD Protected

SYMBOL



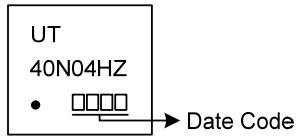
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT40N04HZL-P3030-R	UT40N04HZG-P3030-R	PDFN3x3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

UT40N04HZG-P3030-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) P3030: PDFN3x3
		(3) Green Package	(3) G: Halogen Free and Lead Free, K: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	40	A
	Pulsed (Note 2)	I_{DM}	80	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	60	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.9	V/ns
Power Dissipation		P_D	22	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 34.6\text{A}$, $V_{DD} = 20\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, $T_J \leq T_{JMAX}$, $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	75	$^{\circ}\text{C}/\text{W}$
Junction to Case		θ_{JC}	5.68	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

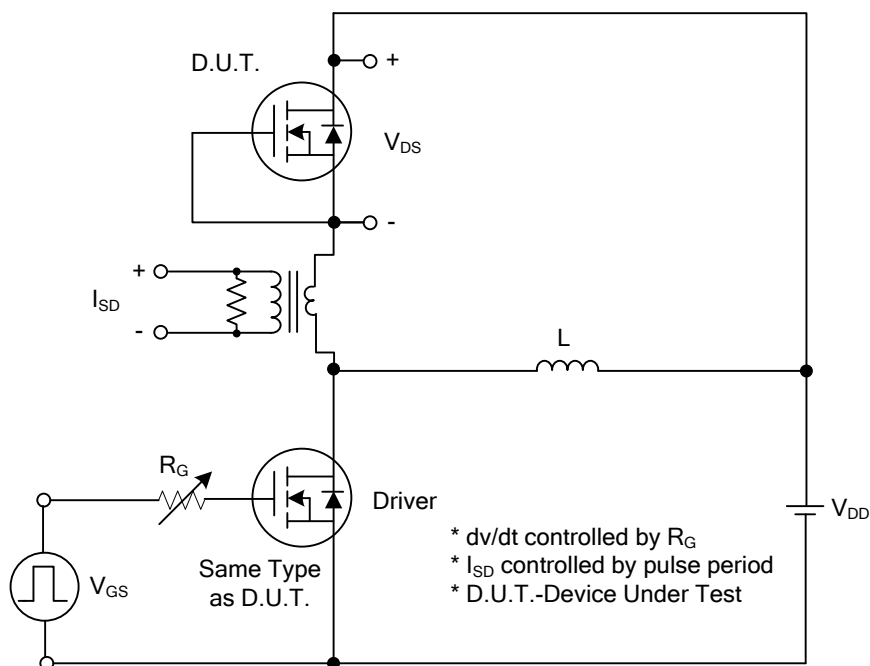
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+10	μA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A			10	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		1412		pF
Output Capacitance		C _{OSS}			184		pF
Reverse Transfer Capacitance		C _{RSS}			152		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =32V, V _{GS} =10V, I _D =40A		47		nC
Gate to Source Charge		Q _{GS}			5		nC
Gate to Drain Charge		Q _{GD}			20		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =20V, V _{GS} =10V, I _D =40A, R _G =3Ω		7		ns
Rise Time		t _R			17		ns
Turn-OFF Delay Time		t _{D(OFF)}			130		ns
Fall-Time		t _F			71		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				40	A
Maximum Body-Diode Pulsed Current		I _{SM}				80	A
Drain-Source Diode Forward Voltage		V _{SD}	I _{SD} =40A			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =30A, dI/dt=100A/μs		56		ns
Body Diode Reverse Recovery Charge		Q _{rr}			57		nC

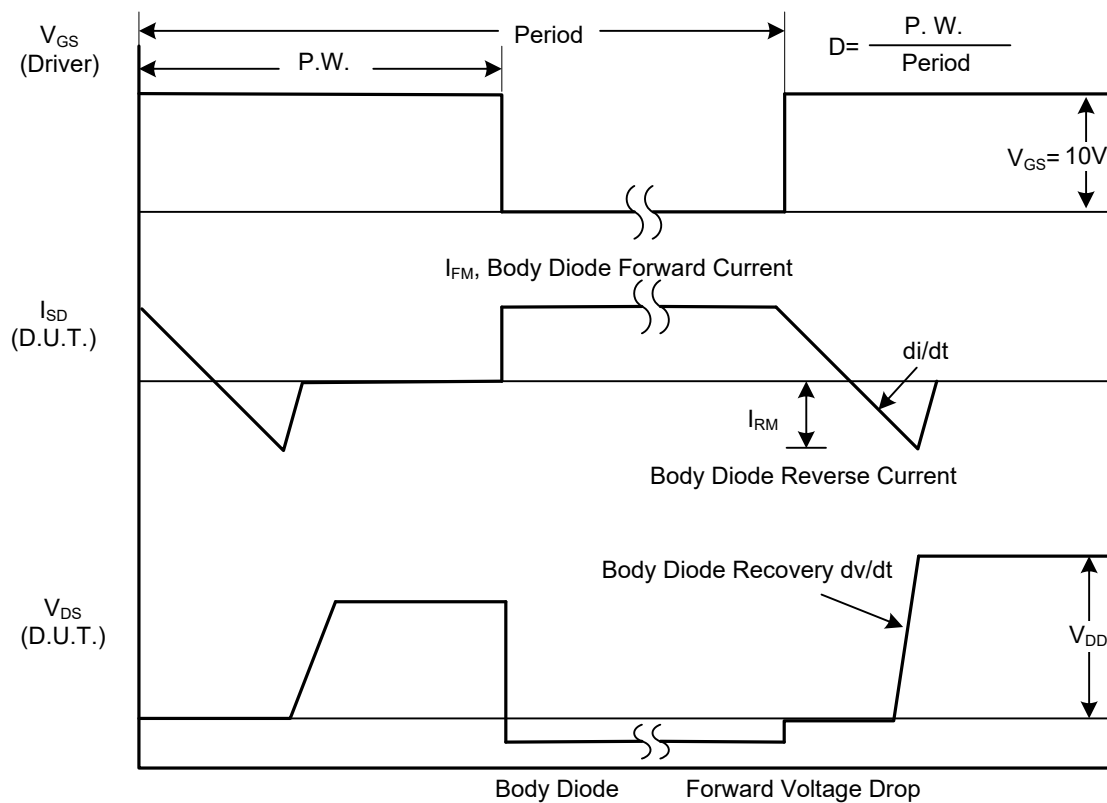
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

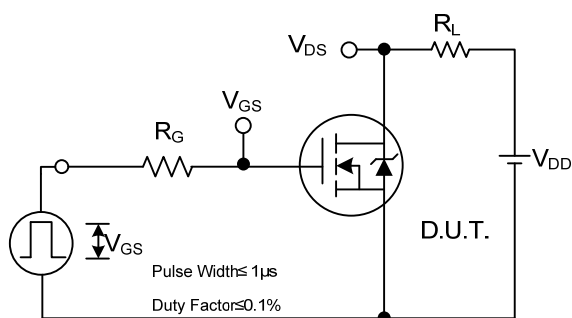


Peak Diode Recovery dv/dt Test Circuit

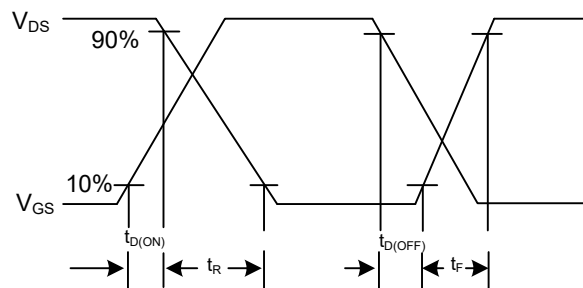


Peak Diode Recovery dv/dt Waveforms

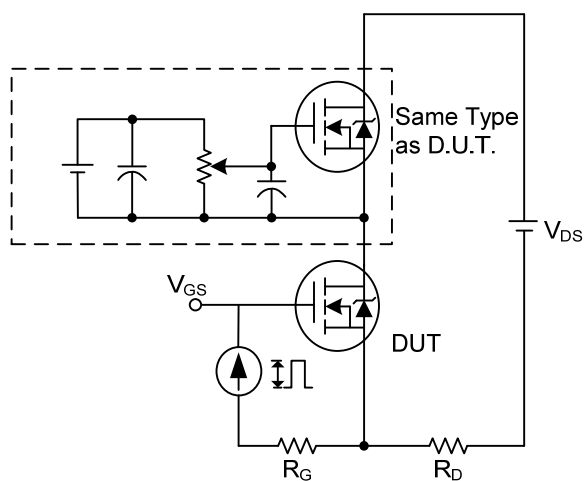
■ TEST CIRCUITS AND WAVEFORMS



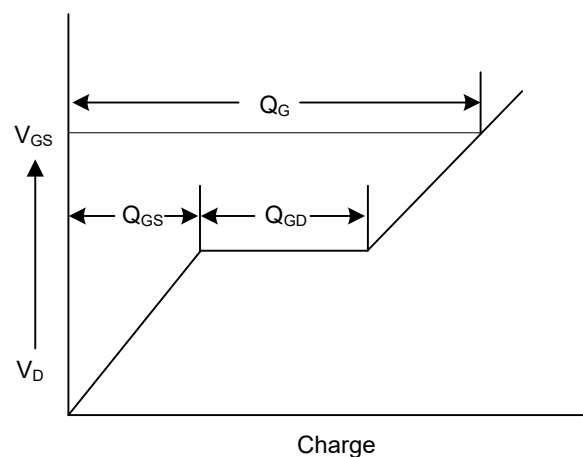
Switching Test Circuit



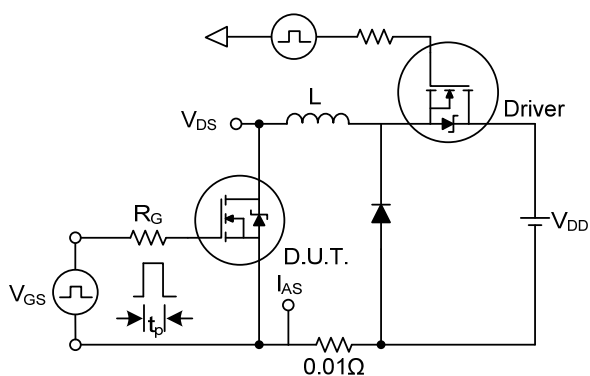
Switching Waveforms



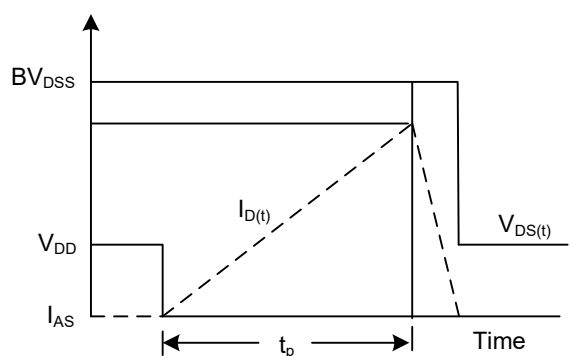
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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