

**UT2013**

Preliminary

POWER MOSFET**10.5A, 20V N-CHANNEL
ENHANCEMENT MODE
MOSFET****DESCRIPTION**

The UTC **UT2013** is a N-channel Power MOSFET, designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

FEATURES

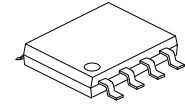
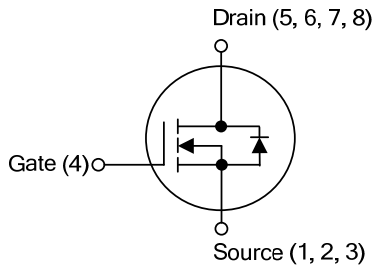
* $R_{DS(ON)} \leq 11 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=8.5\text{A}$

$R_{DS(ON)} \leq 15 \text{ m}\Omega$ @ $V_{GS}=2.5\text{V}$, $I_D=8.5\text{A}$

$R_{DS(ON)} \leq 25 \text{ m}\Omega$ @ $V_{GS}=1.8\text{V}$, $I_D=1.0\text{A}$

$R_{DS(ON)} \leq 50 \text{ m}\Omega$ @ $V_{GS}=1.5\text{V}$, $I_D=0.5\text{A}$

* Low $R_{DS(ON)}$ – Ensures On-State Losses Are Minimized

SYMBOL

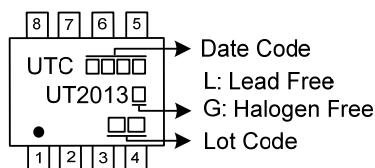
SOP-8

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT2013L-S08-R	UT2013G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT2013G-S08-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) S08: SOP-8
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

■ **ABSOLUTE MAXIMUM RATING** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	V
Drain Current	Continuous	I_D	10.5	A
	Pulsed (Note 2)	I_{DM}	21	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	50.5	mJ
Power Dissipation		P_D	1.6	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 31.8\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	90	$^{\circ}\text{C/W}$
Junction to Case	θ_{JC}	78	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

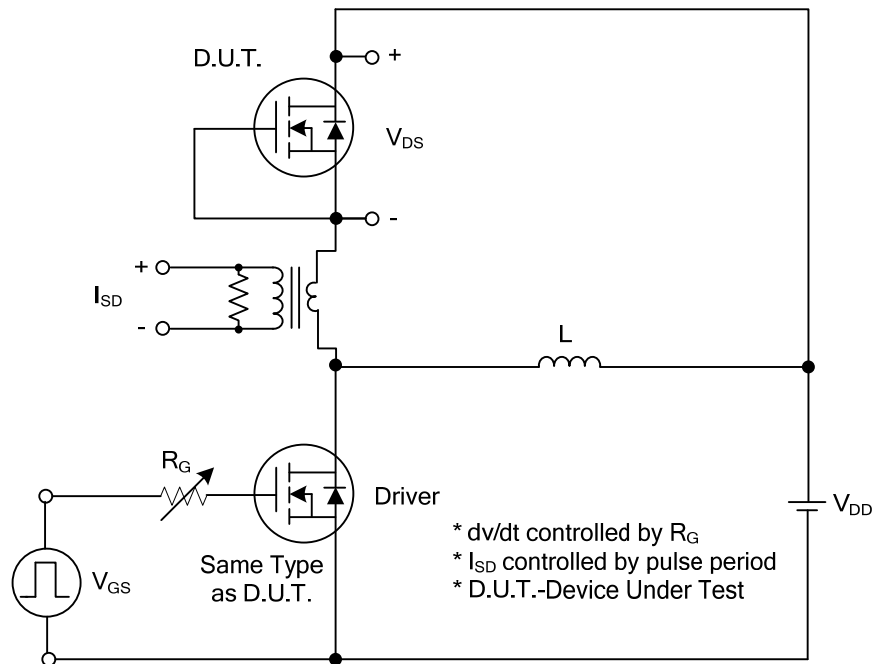
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	20			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+8V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-8V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	0.4		1.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =4.5V, I _D =8.5A			11	mΩ
			V _{GS} =2.5V, I _D =8.5A			15	mΩ
			V _{GS} =1.8V, I _D =1.0A			25	mΩ
			V _{GS} =1.5V, I _D =0.5A			50	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =15V, f=1.0MHz		900		pF
Output Capacitance		C _{OSS}			250		pF
Reverse Transfer Capacitance		C _{RSS}			216		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G (V _{GS} =8V)	V _{DS} =18V, I _D =10.5A, (Note 1, 2)		33		nC
		Q _G (V _{GS} =4.5V)			21		nC
Gate to Source Charge		Q _{GS}			2		nC
Gate to Drain Charge		Q _{GD}			10		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DD} =10V, V _{GS} =4.5V, I _D =10.5A, R _G =3Ω (Note 1, 2)		5		ns
Rise Time		t _R			16		ns
Turn-off Delay Time		t _{D(OFF)}			27		ns
Fall-Time		t _F			23		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				10.5	A
Maximum Body-Diode Pulsed Current		I _{SM}				21	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =10.5A, V _{GS} =0V			1.4	V

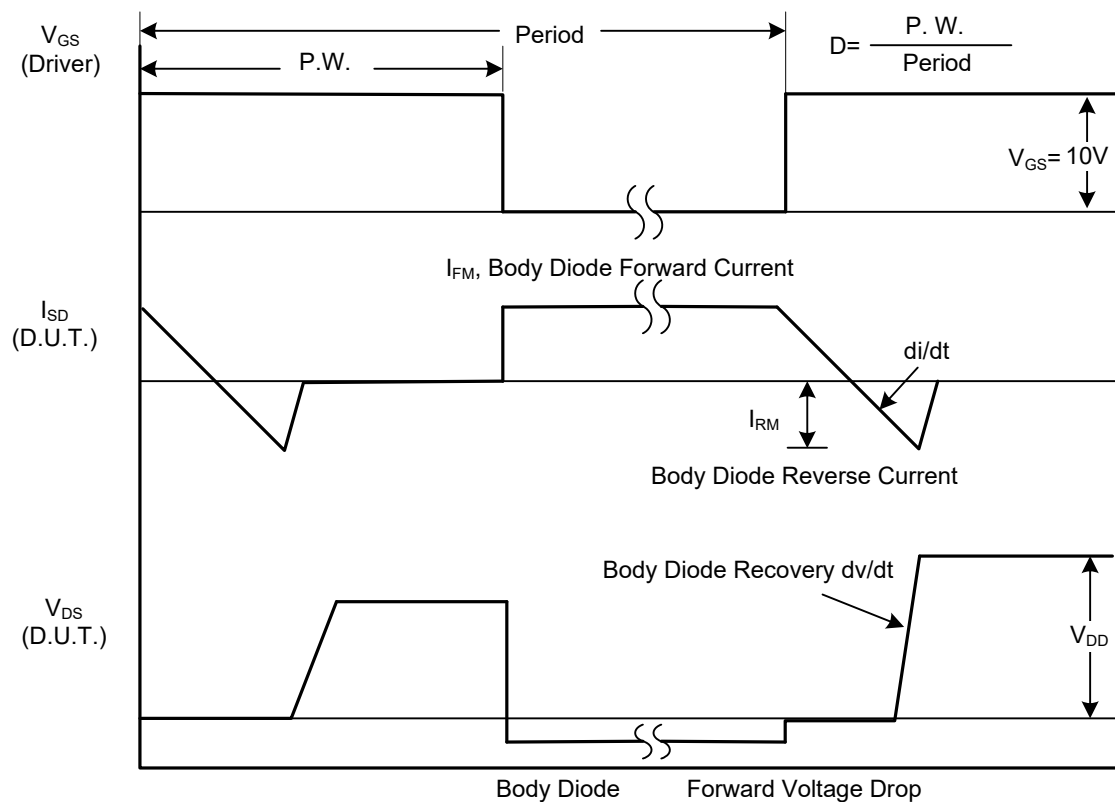
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



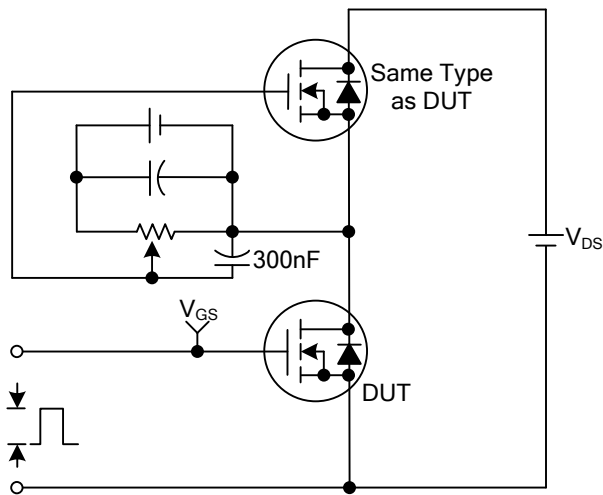
Peak Diode Recovery dv/dt Test Circuit



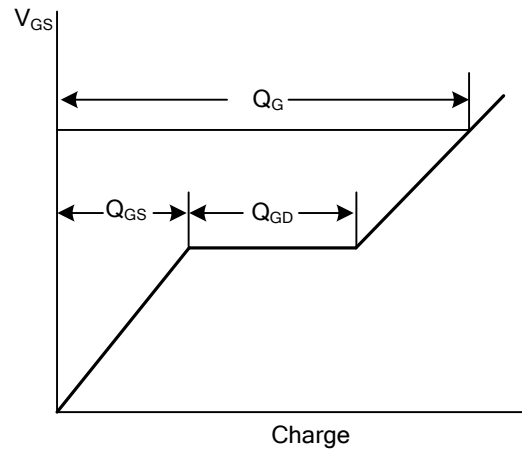
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

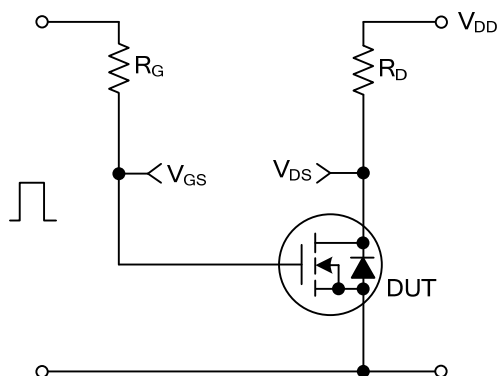
Gate Charge Test Circuit



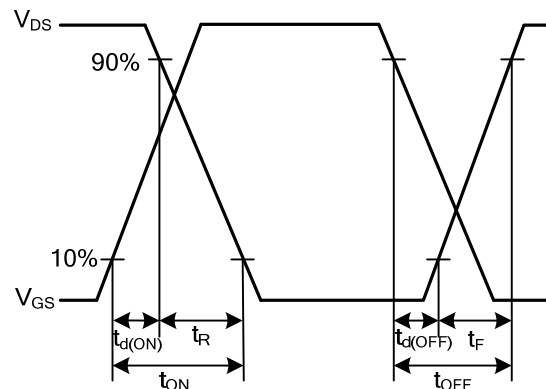
Gate Charge Waveforms



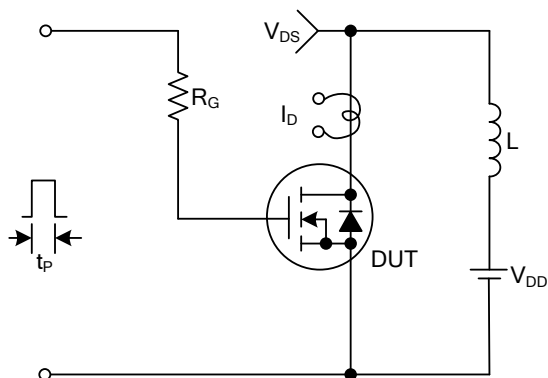
Resistive Switching Test Circuit



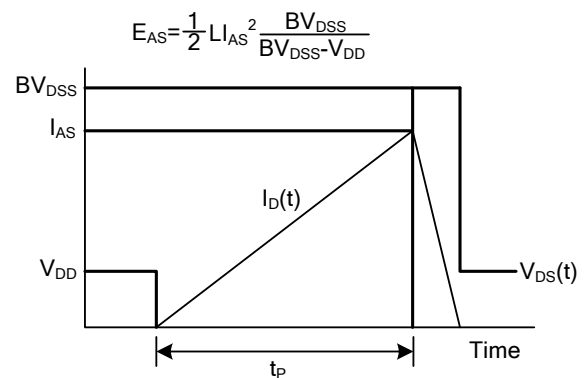
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



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