

# UNISONIC TECHNOLOGIES CO., LTD

### UT8205K

Preliminary

**POWER MOSFET** 

## 6.0A, 20V N-CHANNEL POWER MOSFET

#### DESCRIPTION

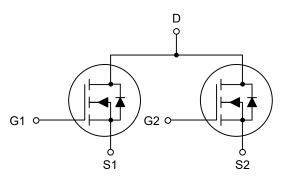
The **UT8205K** uses advanced technology to provide fast switching, low on-resistance and cost-effectiveness. This device is suitable for all commercial-industrial surface mount applications.

#### FEATURES

- \*  $R_{DS(ON)} \le 23 \text{ m}\Omega @ V_{GS}=4.5V, I_D=6.0A$
- $R_{DS(ON)} \le 31 \text{ m}\Omega @ V_{GS}=2.5V, I_D=5.2A$
- \* Fast switching capability
- \* Avalanche energy Specified
- \* Improved dv/dt capability, high ruggedness

## 6 6 1 2 3 SOT-26

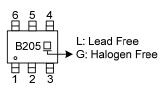
#### SYMBOL



#### ORDERING INFORMATION

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Ordering Number		Deekere	Pin Assignment						De alciere
Lead Free	Halogen Free	Package 1 2 3 4		5	6	Packing			
UT8205KL-AG6-R	UT8205KG-AG6-R	SOT-26	S1	D	S2	G2	D	G1	Tape Reel
Note: Pin Assignment: D: Drain G: Gate S: Source									
UT8205KG-AG6-R		(1) R: Tape Reel (2) AG6: SOT-26							
	(3) G: Halogen Free and Lead Free, L: Lead Free								

#### ■ MARKING



#### ■ ABSOLUTE MAXIMUM RATING (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V <sub>DSS</sub>	20	V	
Gate-Source Voltage		V <sub>GSS</sub>	±8	V	
Drain Current	Continuous	ID	6	А	
	Pulsed	I <sub>DM</sub>	20	А	
Avalanche energy	Single Pulsed (Note 3)	E <sub>AS</sub>	10	mJ	
Power Dissipation		PD	1.14	W	
Junction Temperature		TJ	+150	°C	
Storage Temperature Range		T <sub>STG</sub>	-55 ~ +150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

- 3. L = 0.1mH,  $I_{AS}$  = 14.1A,  $V_{DD}$  = 30V,  $R_{G}$  = 25 $\Omega$  Starting  $T_{J}$  = 25 $^{\circ}$ C
- 4.  $I_{SD} \le 6A$ , di/dt  $\le 200A/\mu$ s,  $V_{DD} \le BV_{DSS}$ , Starting  $T_J = 25^{\circ}C$

#### THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	110	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

#### ■ ELECTRICAL CHARACTERISTICS (TJ=25°C, unless otherwise specified)

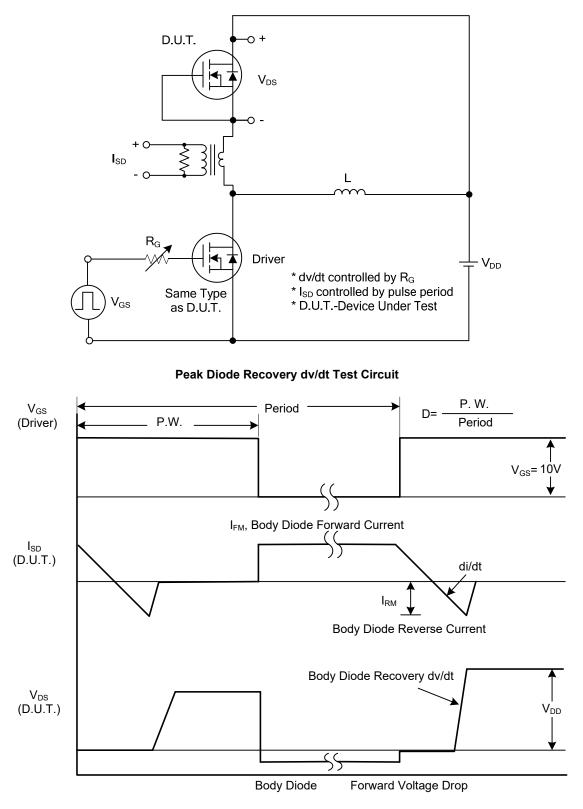
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	I <sub>D</sub> =250µA, V <sub>GS</sub> =0V	20			V
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	μA
Posta Davina La chana Davina f	Forward	Igss	V <sub>GS</sub> =+8V, V <sub>DS</sub> =0V			+100	nA
Gate-Source Leakage Current	Reverse		V <sub>GS</sub> =-8V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	0.5		1.5	V
Static Drain-Source On-State Resistance			V <sub>GS</sub> =4.5V, I <sub>D</sub> =6.0A			23	mΩ
		Rds(on)	V <sub>GS</sub> =2.5V, I <sub>D</sub> =5.2A			31	mΩ
DYNAMIC CHARACTERISTICS							
put Capacitance		CISS			490		pF
Output Capacitance		Coss	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		81		pF
Reverse Transfer Capacitance		C <sub>RSS</sub>			65		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		$Q_{G}$			20		nC
Gate to Source Charge		Q <sub>GS</sub>	$V_{DS}$ =16V, $V_{GS}$ =10V, $I_{D}$ =6.0A		2		nC
Gate to Drain Charge		$Q_{GD}$	(Note 1, 2)		3		nC
Turn-on Delay Time (Note 1)		t <sub>D(ON)</sub>			4		ns
Rise Time		t <sub>R</sub>	V <sub>DD</sub> =10V, V <sub>GS</sub> =10V, I <sub>D</sub> =6.0A, R <sub>G</sub> =3Ω (Note 1, 2)		16		ns
Turn-off Delay Time		t <sub>D(OFF)</sub>			91		ns
Fall-Time		t⊧			55		ns
SOURCE- DRAIN DIODE RATINGS	AND CH	ARACTERIS	TICS				
Maximum Body-Diode Continuous Current		ls				6	Α
Drain-Source Diode Forward Voltage (Note 1)		V <sub>SD</sub>	I <sub>S</sub> =6.0A, V <sub>GS</sub> =0V			1.2	V
Notoo: 1. Dulao Toot: Dulao width < 2				•		-	

Notes: 1. Pulse Test: Pulse width  $\leq$  300µs, Duty cycle  $\leq$  2%.

2. Essentially independent of operating temperature.



#### TEST CIRCUITS AND WAVEFORMS

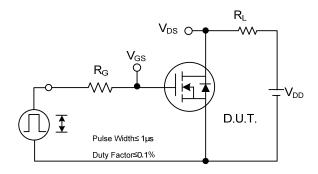


Peak Diode Recovery dv/dt Waveforms

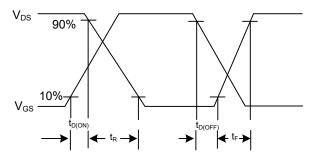


 $V_{GS}$ 

#### TEST CIRCUITS AND WAVEFORMS



Switching Test Circuit

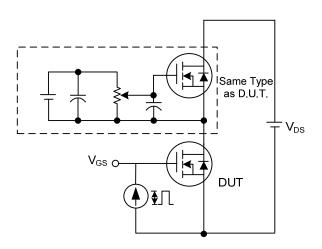


Switching Waveforms

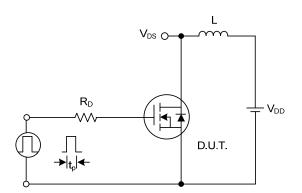
 $\mathsf{Q}_{\mathsf{G}}$ 

Q<sub>GD</sub>-

Q<sub>GS</sub>-



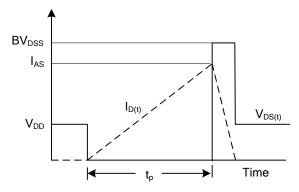
Gate Charge Test Circuit

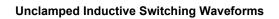


**Unclamped Inductive Switching Test Circuit** 

Gate Charge Waveform

Charge







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