

U74LVC245B

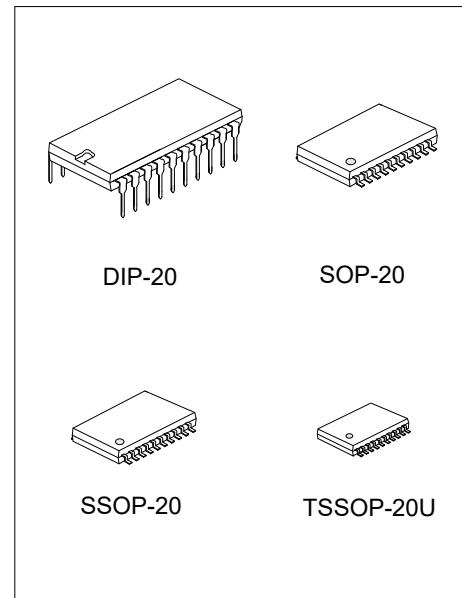
Preliminary

CMOS IC**OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS****■ DESCRIPTION**

The **U74LVC245B** is designed for the communication between data buses asynchronously. While the direction-control(DIR) is high, data transmits from the A bus to the B bus. Data transmits from the B bus to the A bus if DIR is low. The output-enable(\overline{OE}) will isolate the device from the buses when high voltage is applied on it.

■ FEATURES

- * Operate From 1.65V to 3.6V
- * Input Accept Voltages to 5.5V
- * Partial-Power-Down Mode Operation

**■ ORDERING INFORMATION**

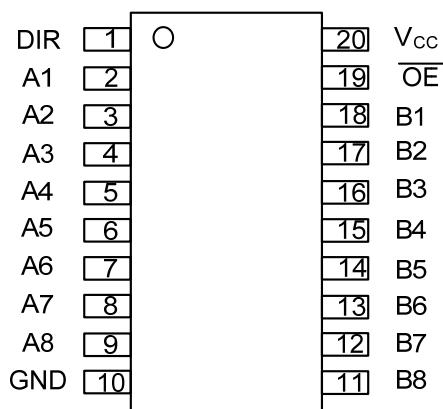
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC245BL-D20-T	U74LVC245BG-D20-T	DIP-20	Tube
U74LVC245BL-S20-R	U74LVC245BG-S20-R	SOP-20	Tape Reel
U74LVC245BL-R20-R	U74LVC245BG-R20-R	SSOP-20	Tape Reel
U74LVC245BL-ULA-R	U74LVC245BG-ULA-R	TSSOP-20U	Tape Reel

 U74LVC245BG-D20-T	(1)T: Tube, R: Tape Reel (2)D20: DIP-20, S20: SOP-20, R20: SSOP-20 ULA: TSSOP-20U (3)G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING

DIP-20	SOP-20 / SSOP-20 / TSSOP-20U
 20 19 18 17 16 15 14 13 12 11 UTC Date Code U74LVC245B L: Lead Free Lot Code 1 2 3 4 5 6 7 8 9 10	 20 19 18 17 16 15 14 13 12 11 UTC Date Code U74LVC245B L: Lead Free G: Halogen Free Lot Code 1 2 3 4 5 6 7 8 9 10

■ PIN CONFIGURATION

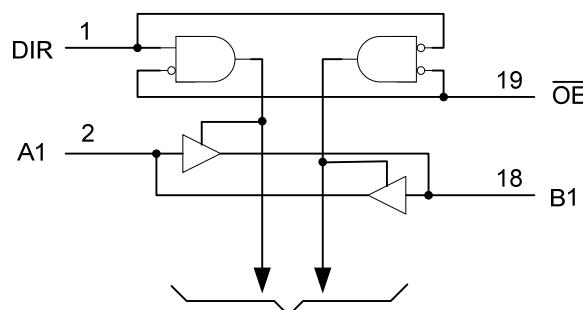


■ FUNCTION TABLE (each gate)

INPUT		FUNCTION
\overline{OE}	DIR	
H	X	Isolation
L	H	Transmit data from A bus to B bus
L	L	Transmit data from B bus to A bus

H = High voltage level ; L = Low voltage level ; X = Don't care

■ LOGIC DIAGRAM (positive logic)



Seven Other Channels

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 6.5	V
Input Voltage	V_{IN}		-0.5 ~ 6.5	V
Voltage Applied To Output In High-Impedance or Power-off State	V_{OUT}		-0.5 ~ 6.5	V
Voltage Applied to Output In High or Low State			-0.5 ~ $V_{CC}+0.5$	V
Input Clamp Current	I_{IK}	$V_{IN} < 0$	-50	mA
Output Clamp Current	I_{OK}	$V_{OUT} < 0$	-50	mA
Output Current	I_{OUT}	$V_{OUT} = 0 \sim V_{CC}$	± 50	mA
V_{CC} or GND Current	I_{CC}		± 100	mA
Storage Temperature	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-20	75	°C/W
	SOP-20	100	°C/W
	SSOP-20	115	°C/W
	TSSOP-20U	120	°C/W
	θ_{JA}		

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage High-Level	V _{IH}	V _{CC} = 1.65V to 1.95V	0.65 ×V _{CC}			0.65 ×V _{CC}			V
		V _{CC} = 2.3V to 2.7V	1.7			1.7			V
		V _{CC} = 2.7V to 3.6V	2			2			V
Input Voltage Low-Level	V _{IL}	V _{CC} = 1.65V to 1.95V			0.35 ×V _{CC}			0.35 ×V _{CC}	V
		V _{CC} = 2.3V to 2.7V			0.7			0.7	V
		V _{CC} = 2.7V to 3.6V			0.8			0.8	V
Output Voltage High-Level	V _{OH}	V _{CC} =1.65V to 3.6V, I _{OH} = -100μA	V _{CC} -0.2			V _{CC} -0.3			V
		V _{CC} =1.65V, I _{OH} = -4mA	1.29			1.05			V
		V _{CC} =2.3V, I _{OH} = -8mA	1.9			1.6			V
		V _{CC} =2.7V, I _{OH} = -12mA	2.2			2.05			V
		V _{CC} =3V, I _{OH} = -12mA	2.4			2.25			V
		V _{CC} =3V, I _{OH} = -24mA	2.3			2.0			V
Output Voltage Low-Level	V _{OL}	V _{CC} =1.65V to 3.6V, I _{OL} =100μA			0.1			0.3	V
		V _{CC} =1.65V, I _{OL} = 4mA			0.24			0.65	V
		V _{CC} =2.3V, I _{OL} = 8mA			0.3			0.8	V
		V _{CC} =2.7V, I _{OL} = 12mA			0.4			0.6	V
		V _{CC} =3V, I _{OL} = 24mA			0.55			0.8	V
Input Leakage Current	I _(LEAK)	V _{CC} =3.6V V _{IN} = 5.5V or GND			±1			±20	μA
Power OFF Leakage Current	I _{OFF}	V _{CC} =0V, V _{IN} or V _{OUT} =5.5V			±1			±20	μA
Input Leakage Current (For I/O Ports)	I _{OZ}	V _{CC} =3.6V, V _{OUT} = 0~5.5V			±1			±20	μA
Quiescent Supply Current	I _Q	V _{CC} =3.6V, V _{IN} =V _{CC} or GND, I _{OUT} =0			1			40	μA
		V _{CC} =3.6V, 3.6V≤V _{IN} ≤5.5V, I _{OUT} =0			1			30	μA
Additional Quiescent Supply Current	ΔI _Q	V _{CC} =2.7V to 3.6V, One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			500			5000	μA

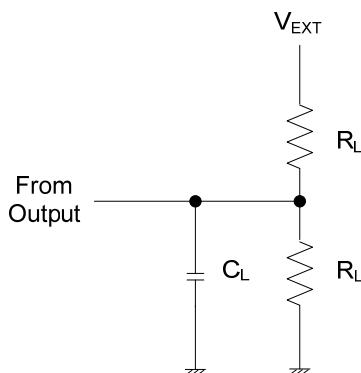
■ SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From A to B or B to A	t _{PLH/t_{PHL}}	V _{CC} =1.8V ± 0.15V	1		11.2			15.9	ns
		V _{CC} =2.5V ± 0.2V	1		6.8			7.7	ns
		V _{CC} =2.7V	1		6.1			8.5	ns
		V _{CC} =3.3V ± 0.3V	1.5		5.1			7	ns
Propagation Delay From OE to A or B	t _{PZL/t_{PZH}}	V _{CC} =1.8V ± 0.15V	1		14			16.5	ns
		V _{CC} =2.5V ± 0.2V	1		9			11.4	ns
		V _{CC} =2.7V	1		8.3			11	ns
		V _{CC} =3.3V ± 0.3V	1.5		7.3			10	ns
Propagation Delay From OE to A or B	t _{PLZ/t_{PHZ}}	V _{CC} =1.8V ± 0.15V	1		15.5			13.2	ns
		V _{CC} =2.5V ± 0.2V	1		8			10	ns
		V _{CC} =2.7V	1		7.3			9	ns
		V _{CC} =3.3V ± 0.3V	1.7		6.3			8	ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	$V_{CC}=3.3V, V_{IN} = V_{CC}$ or GND		3.8		pF
Power Dissipation Capacitance	C_{PD}	$\bar{OE} = 0, f=10MHZ, V_{CC}=1.8V$		42		pF
		$\bar{OE} = 0, f=10MHZ, V_{CC}=2.5V$		43		pF
		$\bar{OE} = 0, f=10MHZ, V_{CC}=3.3V$		45		pF
		$\bar{OE} = 1, f=10MHZ, V_{CC}=1.8V$		1		pF
		$\bar{OE} = 1, f=10MHZ, V_{CC}=2.5V$		1		pF
		$\bar{OE} = 1, f=10MHZ, V_{CC}=3.3V$		2		pF

■ TEST CIRCUIT AND WAVEFORMS



V _{CC}	V _{IN}	t _{R/t_F}	V _M	V _△	C _L	R _L	V _{EXT}		
							t _{PLH/t_{PHL}}	t _{PZH/t_{PHZ}}	t _{PZL/t_{PLZ}}
1.8V ±0.15V	V _{CC}	≤2ns	V _{CC} /2	0.15V	30 pF	1 kΩ	OPEN	GND	2×V _{CC}
2.5V ±0.2V	V _{CC}	≤2ns	V _{CC} /2	0.15V	30 pF	500Ω	OPEN	GND	2×V _{CC}
2.7V	2.7 V	≤2.5ns	1.5V	0.3V	50 pF	500Ω	OPEN	GND	6 V
3.3V ±0.3V	2.7 V	≤2.5ns	1.5V	0.3V	50 pF	500Ω	OPEN	GND	6 V

Fig. 1 Load circuitry

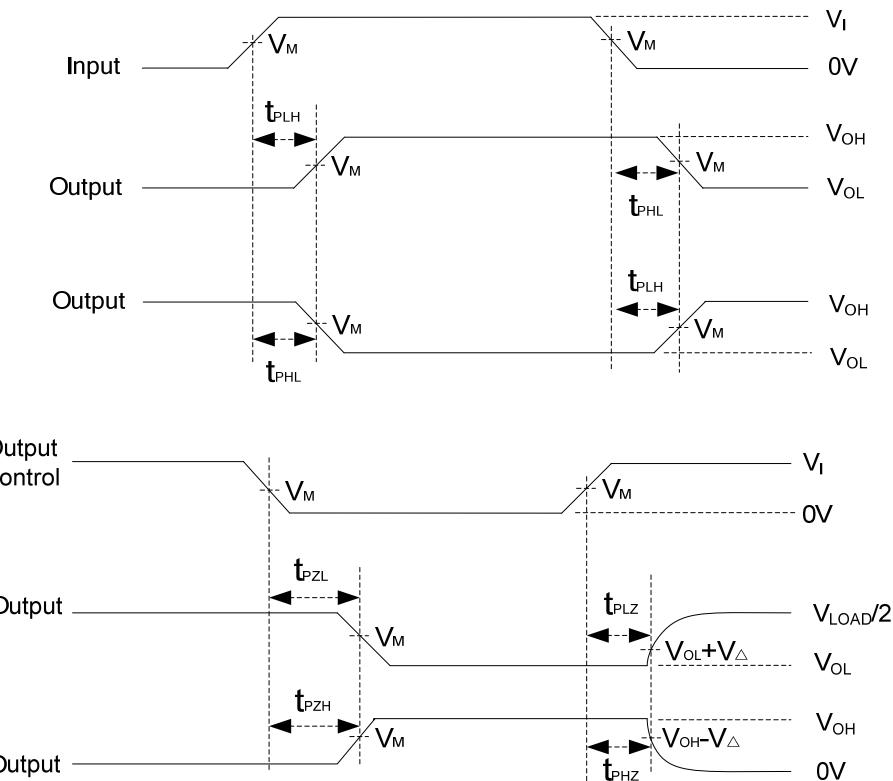


Fig. 2 Propagation delay waves

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