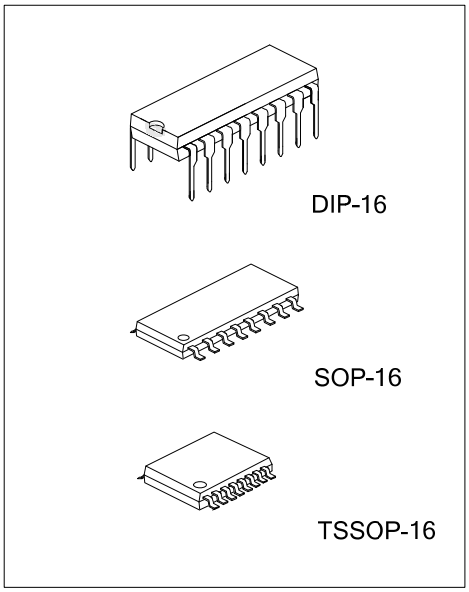
TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



■ DESCRIPTION

UTC **4053A** is triple 2-channel analog multiplexers/demultiplexers for application as digitally–controlled analog switches.

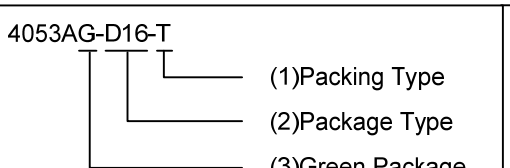
The device has three separate digital control inputs and an inhibit input. It feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

■ FEATURES

* Wide Analog Voltage Range: V_{DD}-V_{EE} = 3V~24V.
  (Note: V_{EE} must be≦V_{SS})
* Break-Before-Make Switching Eliminates Channel Overlap.
* Linearized Transfer Characteristics
* Implement an SPDT Switch Effectively.

■ ORDERING INFORMATION

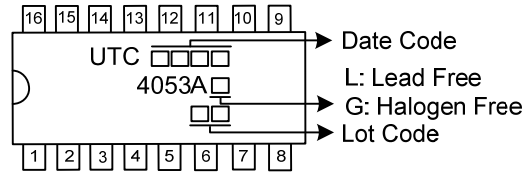
Ordering Number		Package	Packing
Lead Free	Halogen Free		
4053AL-D16-T	4053AG-D16-T	DIP-16	Tube
4053AL-S16-R	4053AG-S16-R	SOP-16	Tape Reel
4053AL-P16-R	4053AG-P16-R	TSSOP-16	Tape Reel



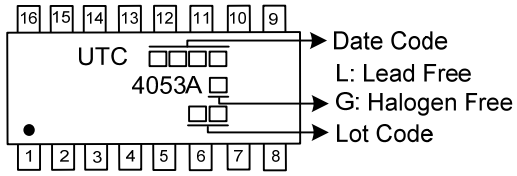
(1) T: Tube, R: Tape Reel
(2) D16: DIP-16, S16: SOP-16, P16: TSSOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

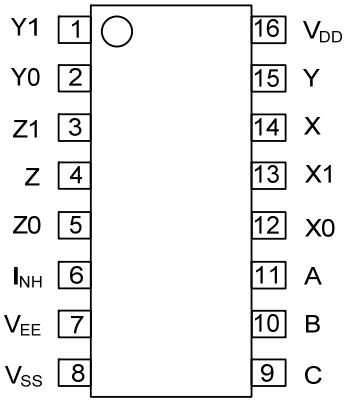
DIP-16



SOP-16 / TSSOP-16



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN No.	SYMBAL	NAME AND FUNCTION
2,1	Y0, Y1	B-Y Switches Inputs/Outputs
5,3	Z0, Z1	C-Z Switches Inputs/Outputs
14,15,4	X,Y,Z	Commons Input/Output
6	INH	Inhibit Input
7	V_{EE}	Supply Voltage
8	V_{SS}	Ground
11,10,9	A,B,C	Digital Control Inputs
12,13	X0, X1	A-X Switches Inputs/Outputs
16	V_{DD}	Positive Supply Voltage

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geqq V_{EE}$)	V_{DD}	-0.5 ~ +24	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{IN}, V_{OUT}	-0.5 ~ V_{DD} +0.5	V
Input Current (DC or Transient), per Control Pin	I_{IN}	±10	mA
Switch Through Current	I_{SW}	±25	mA
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})							
Power Supply Voltage Range		V_{DD}	$V_{DD} - 3 \geqq V_{SS} \geqq V_{EE}$	3		24	V
Quiescent Current per Package	V_{DD}=5V	I_Q	Control Inputs: V_{IN} = V_{SS} or V_{DD} Switch I/O: $V_{EE} \leqq V_{I/O} \leqq V_{DD}$, $\Delta V_{SW} \leqq 500mV$ (Note 2)			5	μA
	V_{DD}=10V					10	μA
	V_{DD}=15V					20	μA
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})							
Recommended Peak–to–Peak Voltage Into or Out of the Switch		$V_{I/O}$	Channel On or Off	0		V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note2)		ΔV_{SW}	Channel On	0		600	mV
Output Offset Voltage		$V_{O(OFF)}$	V_{IN} = 0V, No Load		10		μV
ON Resistance	V_{DD}=5V	R_{ON}	$\Delta V_{SW} \leqq 500mV$ V_{IN} = V_{IL} or V_{IH} (Control), and V_{IN} = 0 to V_{DD} (Switch)		255	1050	Ω
	V_{DD}=10V				125	500	Ω
	V_{DD}=15V				85	280	Ω
ΔON Resistance Between Any Two Channels in the Same Package	V_{DD}=5V	ΔR_{ON}			28		Ω
	V_{DD}=10V				12		Ω
	V_{DD}=15V				12		Ω
Off–Channel Leakage Current		I_{OFF}	V_{IN} = V_{IL} or V_{IH} (Control) Channel to Channel or Any One Channel, V_{DD}=15V			±100	nA
Capacitance, Switch I/O		$C_{I/O}$	Inhibit = V_{DD}		11		pF
Capacitance, Common O/I		$C_{O/I}$	Inhibit = V_{DD}		12.5		pF
Capacitance, Feedthrough (Channel Off)		$C_{I/O}$	Pins Not Adjacent		0.2		pF
			Pins Adjacent		0.5		Pf
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V_{SS})							
Low Level Input Voltage	V_{DD}=5V	V_{IL}	R_{ON}= per spec, I_{OFF} = per spec			1.5	V
	V_{DD}=10V					3.0	V
	V_{DD}=15V					4.0	V
High Level Input Voltage	V_{DD}=5V	V_{IH}	R_{ON}= per spec, I_{OFF} = per spec	3.5			V
	V_{DD}=10V			7.0			V
	V_{DD}=15V			11			V
Input Leakage Current		I_{LEAK}	V_{IN}= 0 or V_{DD}, V_{DD}=15V			±0.1	μA
Input Capacitance		C_{IN}			5.5		pF

■ DYNAMIC ELECTRICAL CHARACTERISTICS

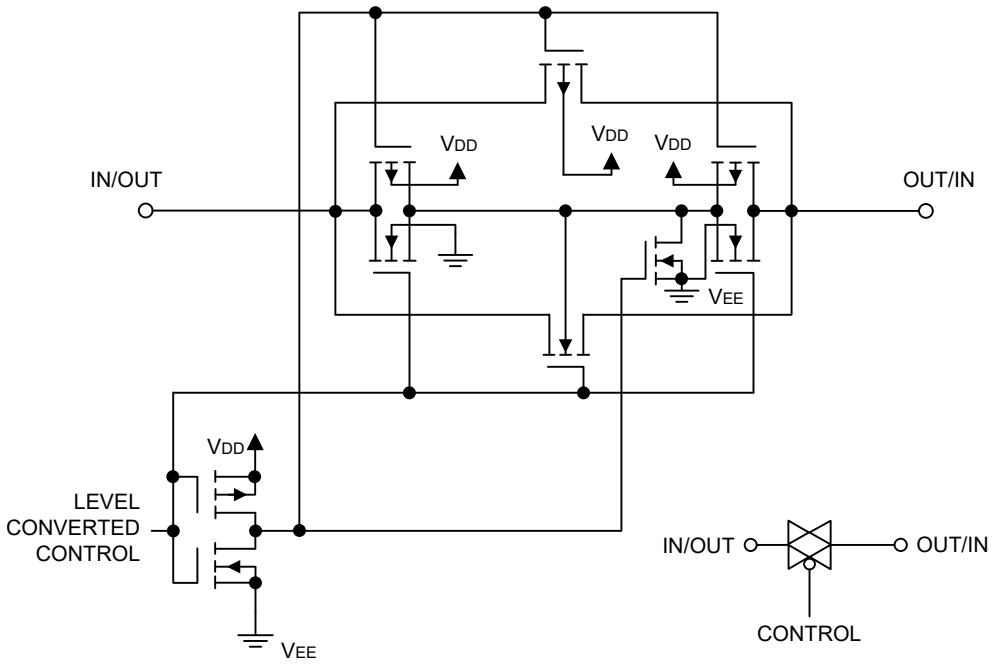
(C_L = 50pF, T_A=25°C, $V_{EE} \leqq V_{SS}$, unless otherwise specified)

PARAMETER	SYMBOL	V_{DD}-V_{EE} V_{DC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Times Switch Input to Switch Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}	5	t_{PLH}, t_{PHL} =(0.17 ns/pF)C_L + 16.5ns		26	65	ns
		10	t_{PLH}, t_{PHL} =(0.08 ns/pF)C_L + 4.0ns		8.5	20	ns
		15	t_{PLH}, t_{PHL} =(0.06 ns/pF)C_L + 3.0ns		6.3	15	ns
Inhibit to Output	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5	(R_L=10kΩ, V_{EE}=V_{SS}), Output “1” or “0” to High Impedance, or High Impedance to “1” or “0” Level		277	550	ns
		10			148	280	ns
		15			112	220	ns
Control Input to Output	t_{PLH}, t_{PHL}	5	R_L = 10kΩ, V_{EE} = V_{SS}		310	600	ns
		10			123	240	ns
		15			82	160	ns
Total Harmonic Distortion	THD	10	R_L = 10KΩ, f = 1 kHz, V_{IN} = 5 V_{PP}		0.07		%
Bandwidth	BW	10	R_L=1kΩ, V_{IN}= 1/2(V_{DD}-V_{EE}) p-p, C_L =50pF, 20 Log (V_{OUT}/V_{IN})= -3dB)		17		MHz
Off Channel Feedthrough Attenuation		10	R_L=1KΩ, V_{IN} = 1/2(V_{DD}-V_{EE}) p-p f_{IN} = 55MHz		-50		dB
Channel Separation		10	R_L = 1kΩ, V_{IN} = 1/2 V_{DD}-V_{EE})p-p f_{IN} = 3MHz		-50		dB
Crosstalk, Control Input to Common O/I		10	R_1 = 1kΩ, R_L = 10kΩ Control t_{TLH} = t_{THL} = 20ns, Inhibit = V_{SS}		75		mV

Notes: 1. Data of “TYP” is intended as an indication of the IC’s potential performance.

2. For voltage drops across the switch(ΔV_{SW})>600mV (>300mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

■ TEST CIRCUIT

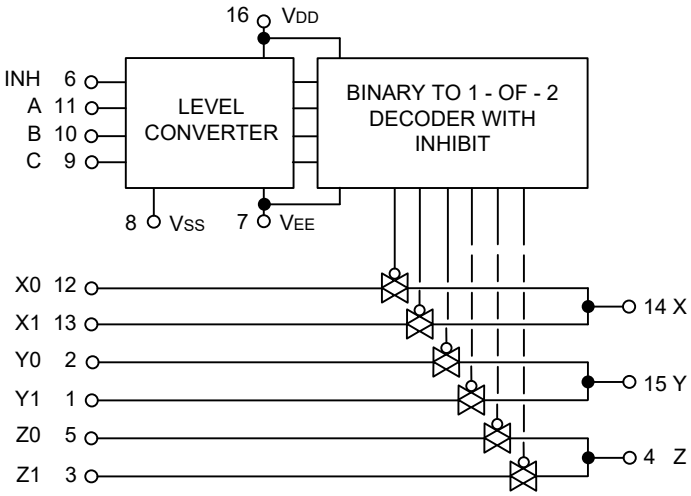


Switch Circuit Schematic

■ TRUTH TABLE

Control Inputs				ON Switches		
INHIBIT	Select					
	C	B	A	UTC **4053A**		
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	None		

x = Don't Care



UTC 4053A Functional Diagram