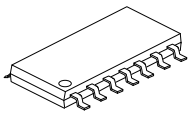
U74HCT164

CMOS IC

HIGH-SPEED CMOS LOGIC 8-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER



SOP-14U

■ DESCRIPTION

The **U74HCT164** is an 8-bit serial-in/parallel-out shift register.

The logical AND of the DSA and DSB enters into Q0 and shifts one place to right on each LOW-to-HIGH transition of the clock (CP). A low level on the master reset ($\overline{MR}$) input clears all the registers asynchronously and force all outputs LOW.

■ FEATURES

* Buffered inputs
* Asynchronous reset
* Balanced propagation delay and transition times
* Significant power reduction
* Wide operating temp range: -40°C to +125°C

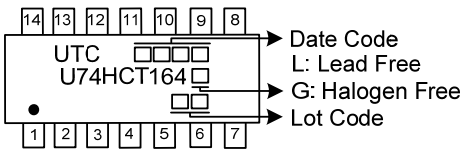
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT164L-UEA-R	U74HCT164G-UEA-R	SOP-14U	Tape Reel

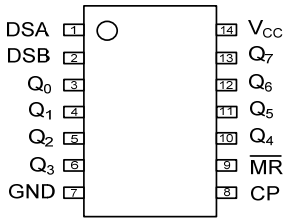
U74HCT164G-UEA-R
- (1)Packing Type
- (2)Package Type
- (3)Green Package

(1) R: Tape Reel
(2) UEA: SOP-14U
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

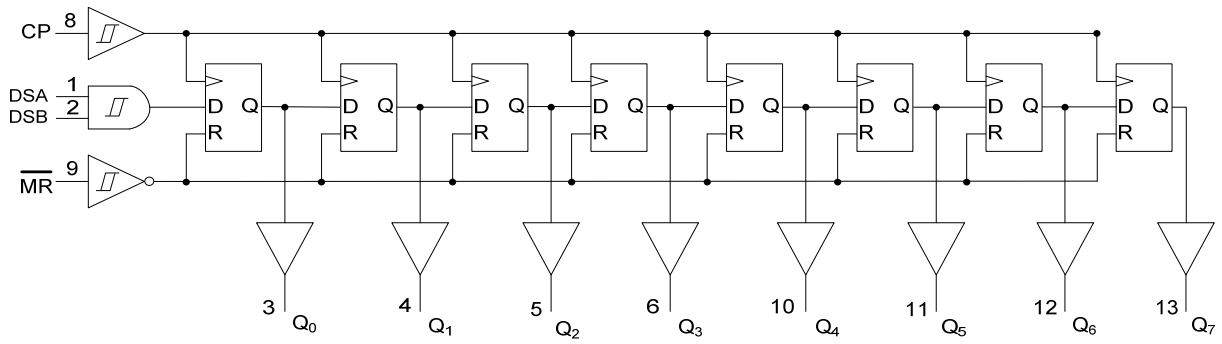


■ FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
RESET (CLEAR)	$\overline{MR}$	CP	DSA	DSB	Q_0	$Q_1 - Q_7$
Shift	L	X	X	X	L	L - L
	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

Notes: H = High voltage level.
L = Low voltage level.
h = High voltage level one set-up time prior to the low-to-high clock transition.
l = Low voltage level one set-up time prior to the low-to-high clock transition.
X = Don't care.
↑ = Transition from low to high level.
q_n = Lower case letters indicate the state of the referenced input one set-up time prior to the low-to-high clock transition.

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7	V
Input Voltage	V_{IN}		0 ~ V_{CC}	V
Output Voltage (Active Mode)	V_{OUT}		0 ~ V_{CC}	V
Input Clamp Current	I_{IK}	V_{IN} < 0V or V_{IN} > V_{CC}	±20	mA
Output Clamp Current	I_{OK}	V_{OUT} < 0V or V_{OUT} > V_{CC}	±20	mA
Continuous Output Current	I_{OUT}	V_{OUT} = 0V to V_{CC}	±25	mA
Continuous Current Through V_{CC} or GND	I_{CC}		±50	mA
Storage Temperature	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise and Fall Time	t_R / t_F	V_{CC}=4.5~5.5V			500	ns
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS (Note 1)	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High Level Input Voltage	V_{IH}	V_{CC}=4.5V~5.5V	2			2			V
Low Level Input Voltage	V_{IL}	V_{CC}=4.5V~5.5V			0.8			0.8	V
High Level Output Voltage	V_{OH}	V_{CC}=4.5V, I_{OH}=-20μA	4.4			4.4			V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98			3.7			V
Low Level Output Voltage	V_{OL}	V_{CC}=4.5V, I_{OL}=20μA			0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=4mA			0.26			0.4	V
Input Leakage Current	I_I	V_{CC}=5.5V, V_I= V_{CC} or GND			±0.1			±1	μA
Supply Current	I_{CC}	V_{CC}=5.5V, V_I= V_{CC} or GND			8			160	μA
Additional Quiescent Supply Current (Note 2, 3)	ΔI_{CC}	V_{CC}=4.5V~5.5V			360			490	uA

Notes: 1. V_I = V_{IH} or V_{IL}, unless otherwise specified.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.
3. Inputs held at V_{CC} – 2.1.

■ TIMING REQUIREMENTS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Clock Frequency	f_{MAX}	V_{CC}=4.5V	27			18			MHz
$\overline{MR}$ Pulse Width	t_W	V_{CC}=4.5V	18			27			ns
CP Pulse Width	t_W	V_{CC}=4.5V	18			27			ns
Set-up Time	t_{SU}	V_{CC}=4.5V	12			18			ns
Hold Time	t_H	V_{CC}=4.5V	4			4			ns
$\overline{MR}$ to Clock Removal Time	t_{REM}	V_{CC}=4.5V	16			24			ns

■ SWITCHING CHARACTERISTICS (t_r, t_f=6ns. C_L=50pF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay from input (CP) to output (Q)	t_{PLH}, t_{PHL}	V_{CC}=4.5V			36			54	ns
		V_{CC}=5V		15 (Note 1)					ns
Propagation delay from input ($\overline{MR}$) to output (Q)	t_{PLH}, t_{PHL}	V_{CC}=4.5V			38			57	ns
		V_{CC}=5V		16 (Note 1)					ns
Output Transition Time	t_{TLH}, t_{THL}	V_{CC}=4.5V			15			22	ns

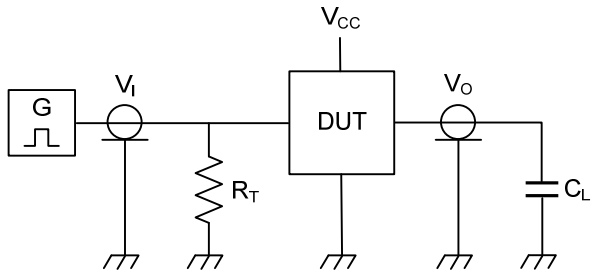
■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}			3.5		pF
Power Dissipation Capacitance (Note 2)	C_{PD}	V_{CC}=5V		49		pF

Notes : 1. C_L=15pF.

2. C_{PD} is used to determine the dynamic power consumption, per device.

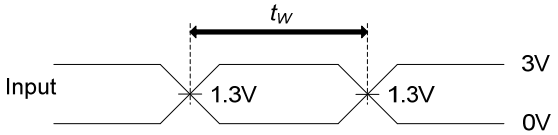
TEST CIRCUIT AND WAVEFORMS



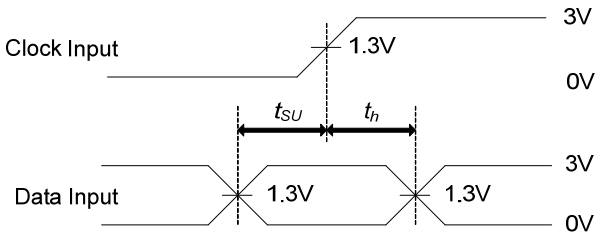
Note: C_L includes probe and jig capacitance.

Table 1. Test Data

TEST	INPUT		Load
	V_I	t_r, t_f	C_L
t_{PLH}, t_{PHL}	3V	6ns	15pF, 50pF



Pulse Duration



Setup Time and Hold Times

Table 2. Measurement points

INPUT	OUTPUT		
V_M	V_M	V_X	V_Y
1.3V	1.3V	0.1 × V_{CC}	0.9 × V_{CC}