

**UT120P04M**

Preliminary

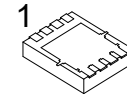
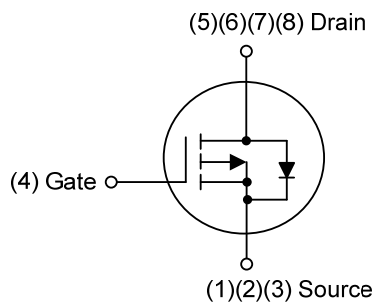
Power MOSFET

**-120A, -40V P-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT120P04M** provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

FEATURES

- * $R_{DS(ON)} \leq 5.2 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -60\text{A}$
- * $R_{DS(ON)} \leq 7.3 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -40\text{A}$
- * 100% Avalanche Tested

SYMBOL

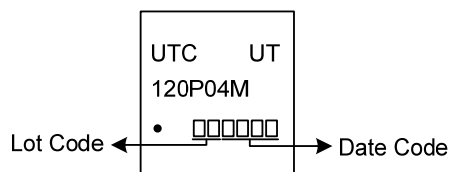
PDFN5×6

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT120P04ML-P5060-R	UT120P04MG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT120P04MG-P5060-R			(1) R: Tape Reel (2) P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free
(1) Packing Type			
(2) Package Type			
(3) Green Package			

MARKING

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous,	I_D	-120	A
	Pulsed (Note 2)	I_{DM}	-240	A
Avalanche Energy	Repetitive (Note 3)	E_{AS}	276	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	0.5	V/ns
Power Dissipation ($T_C=25^{\circ}\text{C}$)		P_D	110	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = -74.2\text{A}$, $V_{DD} = -50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	65	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	1.13	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

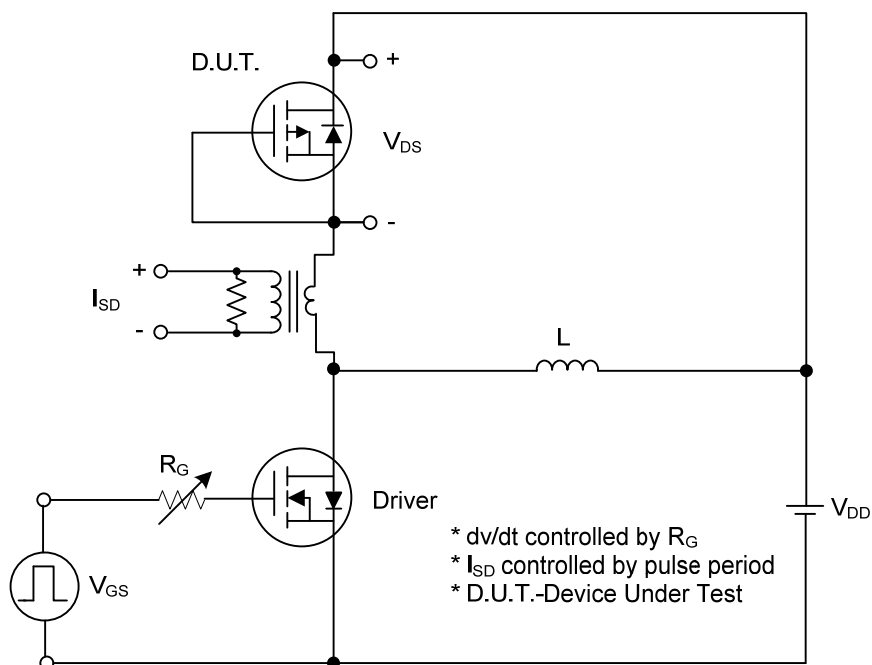
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =-250μA, V _{GS} =0V	-40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-40V, V _{GS} =0V			-1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =-10V, I _D =-60A			5.2	mΩ
			V _{GS} =-4.5V, I _D =-40A			7.3	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =-25V, V _{GS} =0V, f=1MHz		8025		pF
Output Capacitance		C _{OSS}			1030		pF
Reverse Transfer Capacitance		C _{RSS}			495		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =-32V, V _{GS} =-10V, I _D =-120A (Note 1, 2)		209		nC
Gate to Source Charge		Q _{GS}			33		nC
Gate to Drain Charge		Q _{GD}			62		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DS} =-20V, V _{GS} =-10V, I _D =-120A R _G =3Ω (Note 1, 2)		64		ns
Rise Time		t _R			72		ns
Turn-OFF Delay Time		t _{D(OFF)}			1000		ns
Fall-Time		t _F			480		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				-120	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =-120A, V _{GS} =0V (Note 2)			-1.4	V
Body Diode Reverse Recovery Time (Note 1)		t _{rr}	I _S =-30A, V _{GS} =0V,		148		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		433		nC

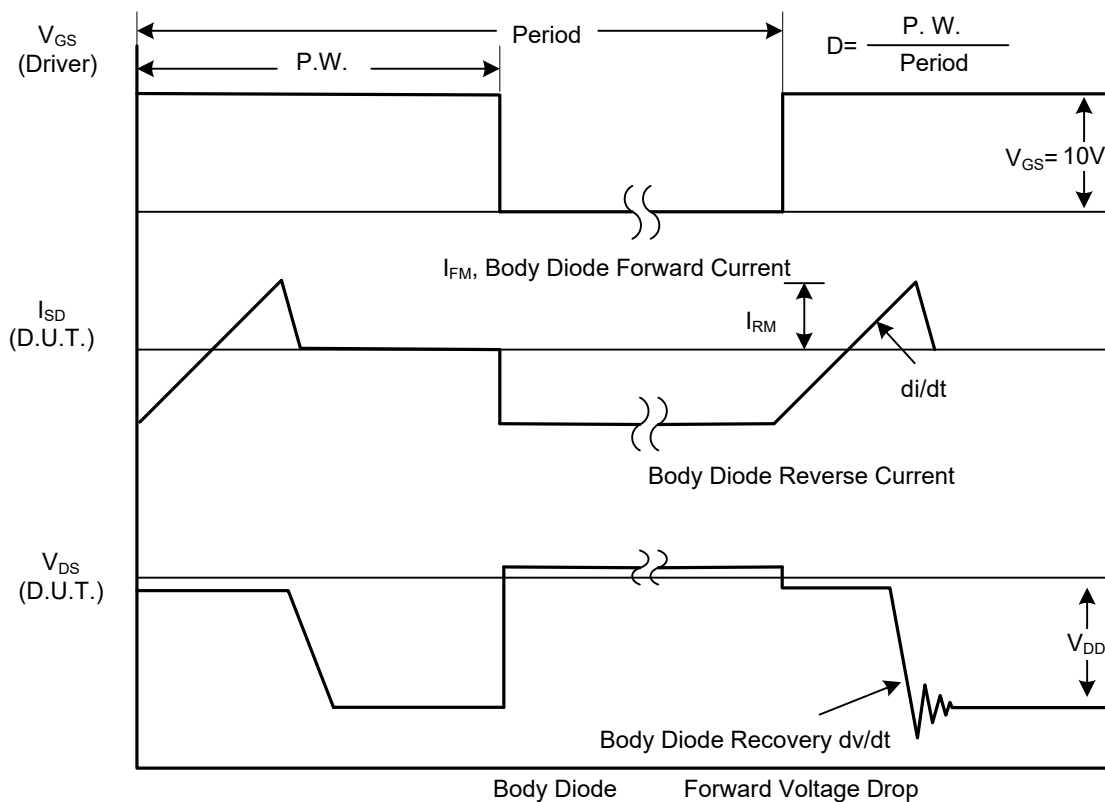
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

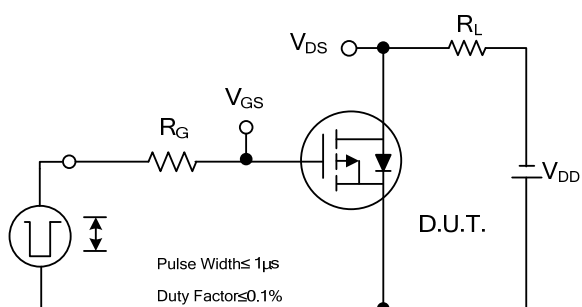


Peak Diode Recovery dv/dt Test Circuit

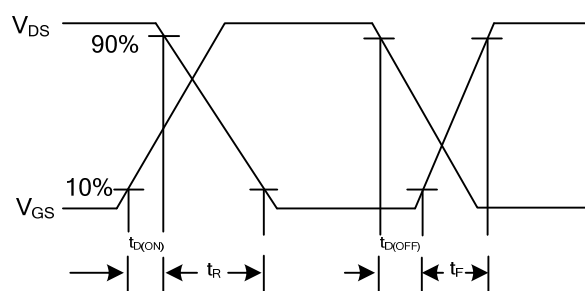


Peak Diode Recovery dv/dt Waveforms

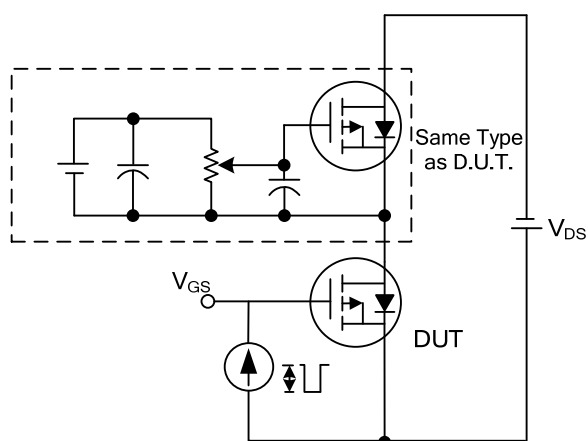
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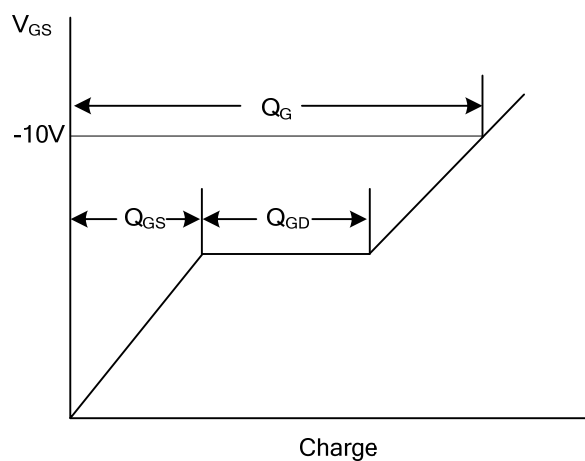
Switching Test Circuit



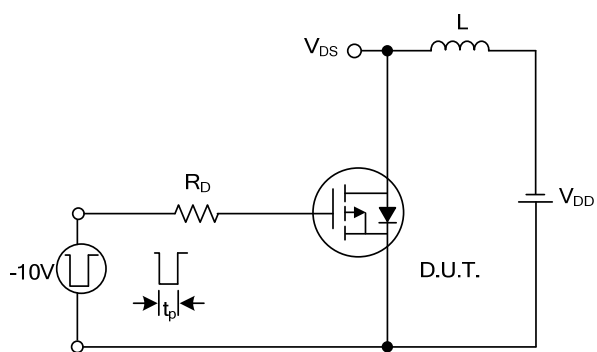
Switching Waveforms



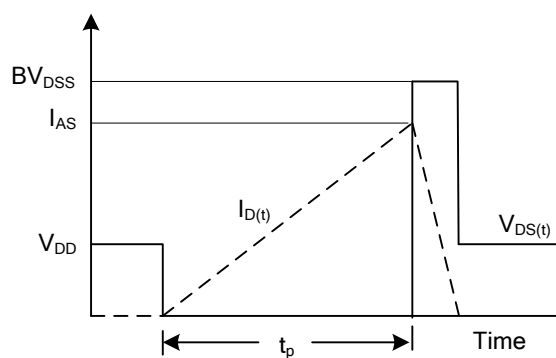
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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