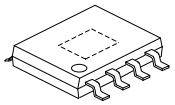
65V, 5A, 520kHz STEP-DOWN CONVERTER WITH LOW-SIDE MOSFET DRIVER AND PROGRAMMABLE FREQUENCY



HSOP-8

■ DESCRIPTION

The UTC **UD65501** is a 65V/5A Step-down converter which is integrated with high-side power MOSFET and low-side driver for external MOSFET.

The **UD65501** can deliver 5A of output current efficiently with constant on time (COT) control for fast loop response.

The **UD65501** achieves high power conversion efficiency over a wide load range by scaling down its switching frequency under light-load conditions to reduce switching and gate driving losses.

The **UD65501** has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open/short protection and thermal shutdown.

The **UD65501** has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open/short protection and thermal shutdown.

■ FEATURES

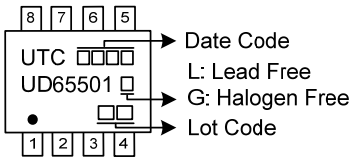
* 4.5V to 65V Wide Input Range
* 5A Continuous Output Current
* Integrated 80mΩ low resistance high side power MOS
* Non-Sync Buck, Sync Buck Selectable by RT/SYNC Pin
* LSG Pin to Drive External LS-FET
* Constant On Time Control with Constant Switching Frequency.
* 130μA Low Quiescent Current
* 250kHz, 500kHz, 1.2MHz, 2.2MHz Switching Frequency Selectable
* External Frequency Synchronization from 200kHz–1.2MHz
* BIAS Pin to improve efficiency
* Low Dropout Mode Support 99.5% Duty Cycle
* Pre-bias Start up

■ ORDERING INFORMATION

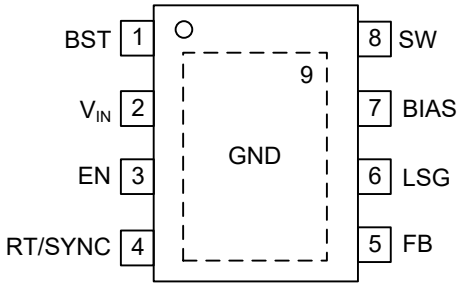
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD65501L-SH2-R	UD65501G-SH2-R	HSOP-8	Tape Reel

UD65501G-SH2-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) SH2: HSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



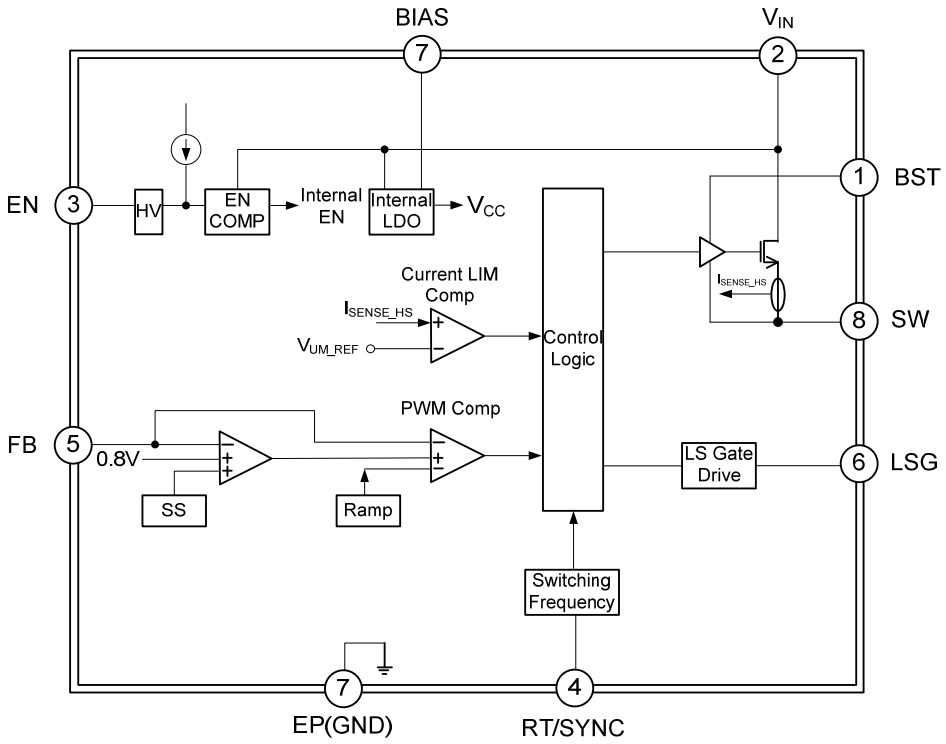
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	PIN	DESCRIPTION
1	BST	O	Bootstrap pin for high side power MOS driving. Connect a high quality capacitor from this pin to the SW pin.
2	V_{IN}	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
3	EN	I	Enable of the part. Pull down this pin to shut down the part. Internally pulled up by a current.
4	RT/SYNC	/	Mode and Frequency Set/External Sync Pin. Place a resistor from RT/SYNC to GND. Choose external diode or MOSFET as low side. IC could work as Non-Sync buck or Sync buck. Also could be used to select the switching frequency 250kHz, 500kHz, 1.2MHz, 2.2MHz. When apply an external clock to RT/SYNC pin can change the switching frequency.
5	FB	I	Feedback. Connect a resistor divider to set the output voltage.
6	LSG		External Low Side MOSFET gate driver. When set up Sync buck, connect LSG pin to external N-MOSFET gate. When set up Non-Sync buck, float this pin.
7	GND	P	External Bias Input of Internal LDO. Connect BIAS to an external power supply (5V ≤ VBIAS ≤ 20V) through a 4.7Ω resistor to reduce power dissipation and increase efficiency. Connect BIAS pin to GND if not use.
8	SW	O	Switching node of power stage. Connect to power inductor.
Exposed Pad	GND	P	Exposed Pad. Connect exposed pad to the PCB GND plane to achieve good thermal performance.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	-0.3 ~ 68	V
SW to GND	V_{SW}	-0.6 (-9V in 10ns) ~ V_{IN} + 0.3 (75V in 10ns)	V
EN to GND	V_{EN}	-0.3 ~ 68	μA
BST to SW	V_{BST-SW}	-0.3 ~ 6	V
BIAS to GND	V_{BIAS}	-0.3 ~ 30	V
LSG to GND	V_{LSG}	-0.3 ~ 10	V
All Other Pins		-0.3 ~ 6	V
Operating Junction Temperature	T_J	-40 ~ +150	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	4.5 ~ 65	V
V_{OUT} to GND	V_{OUT}	0.8 ~ 32	V
BIAS to GND	V_{BIAS}	5 ~ 20	V
Max Continuous Output Current	I_{OUT}	5	A
Junction Temperature	T_J	-40 ~ +125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	48	°C/W
Junction to Case	θ_{JC}	52	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{IN}=48V, V_{OUT}=2V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UVLO AND QUIESCENT CURRENT						
V_{IN} UVLO Rising Threshold	V_{IN_UVR}			4.3		V
V_{IN} UVLO Falling Threshold	V_{IN_UVF}			4.0		V
V_{IN} UVLO Hysteresis	$V_{IN\_UV\_hys}$			0.3		V
Quiescent Supply Current	I_Q	V_{FB} =0.85V		130		μA
Shutdown Current	I_S	V_{EN} = 0V		3		μA
FEEDBACK VOLTAGE						
Feedback Voltage	V_{FB}		0.791	0.803	0.815	V
FB UV Threshold	V_{FB_UV}			0.4		V
OC Hiccup Deglitch Time	T_{OC_DEG}			10		ms
POWER STAGE						
High-Side Switch on Resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		80		mΩ
High-Side Switch on Leakage Current	I_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V			1	μA
CURRENT LIMIT						
High-Side Current Limit Threshold	I_{LIM_HS}			7.5		A
SOFT START						
Internal Soft-Start time	T_{SS}	V_{FB} from 10% to 90%		1.2		ms
SWITCHING FREQUENCY/SYNC FUNCTION						
Non-Sync Buck Switching Frequency	F_{SW}	$R_{RT/SYNC}$ = 0kΩ		2200		kHz
		$R_{RT/SYNC}$ = 91kΩ		1200		kHz
		$R_{RT/SYNC}$ = 180kΩ		500		kHz
		$R_{RT/SYNC}$ = 430kΩ		250		kHz
Sync Buck Switching Frequency (FPWM Mode)		$R_{RT/SYNC}$ = 820kΩ		1200		kHz
		$R_{RT/SYNC}$ = 1.8kΩ		500		kHz
		RT/SYNC Pin Float		250		kHz
External Clock	F_{SYNC}		0.2		1.2	MHz
Min Sync Pulse Width (Note)	T_{SYNC_MIN}			20		ns
SYNC Input Voltage Threshold	V_{IH_SYNC}			1.55	2.0	V
	V_{IL_SYNC}		0.5	1.2		V
Min On pulse (Note)	T_{ON_MIN}			120		ns
Max On pulse (Note)	T_{ON_MAX}			40		μs
Min. OFF Time (Note)	T_{OFF_MIN}	Non-Sync buck		140		ns
ENABLE						
Enable Rising Threshold	V_{EN_RISING}	Low to High		1.2		V
EN Pulled-up Current	$I_{EN\_PULL\_UP}$	EN=High		5		μA
		EN=Low		1.2		μA
EN Pulled-up Current Hysteresis	I_{EN_Hys}			3.8		μA
LSG						
LSG High Level Voltage	V_{LSG}			6.7		V
LSG Source Current	I_{SOURCE}			120		mA
LSG Pull-Down Resistor	R_{LOW}			1.4		Ω
THERMAL PROTECTION						
Thermal Shutdown Entry(Note)	T_{OTP_RISING}			160		°C
Thermal Shutdown Recovery (Note)	$T_{OTP\_FALLING}$			140		°C

Note: Guaranteed by design and engineering sample characterization.

■ FUNCTION DESCRIPTIONS

Pulse-Width Modulation (PWM) Control

The **UD65501** is a step-down, switch-mode converter which is integrated with high-side power MOSFET(HS-FET) and low-side driver for external low-side MOSFET(LS-FET). Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off. The free-wheeling diode or external LS-FET will handle the current. The HS-FET is turned on again when VFB drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Non-Sync Buck Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 1). When V_{FB} is below VREF, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the external free-wheeling diode will handle the current.

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

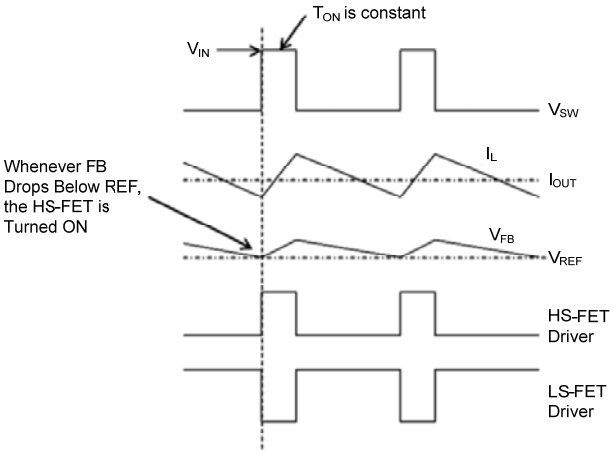


Figure 1. Heavy-Load Operation

■ FUNCTION DESCRIPTIONS (Cont.)

Non-Sync Buck Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM). Light-load operation is shown in Figure 2. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the free-wheeling diode is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The free-wheeling diode will shut down the negative current and IC goes into tri-state. The output capacitor discharge to GND through the feedback resistor slowly. So the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode. High efficiency is achieved in light-load condition.

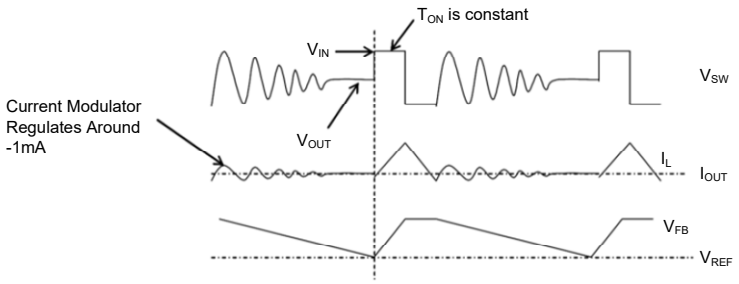


Figure 2. Light-Load Operation

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation shown below:

$$I_{OUT\_Critical} = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{2\times L\times f_{SW}\times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Sync Buck Application

UD65501 has a LSG pin which can be used to drive the external N-MOSFET as the Buck converter LS-FET. If use LSG pin, need to set the resistor between RT/SYNC and GND larger than 800kΩ or float RT/SYNC pin. The whole circuit will work as Sync buck. IC will work in FPWM mode.

In FPWM mode, IC switching frequency is fairly consistent with load current changing, this will help to minimize light-load V_{OUT} ripple, meantime ease the second stage filter design to damp the power stage noise, another side, due to internal power HS-FET on and off more frequently, the light-load efficiency is lower than PFM mode.

When work as Sync buck, an internal 120mA current will charge the external LS-FET gate to high-level voltage 6V (typical). An external LS-FET which's Qg is less than 30nC with 1.4V to 2.5V V_{TH} is recommended to achieve better efficiency. Also recommend to connect BIAS pin to V_{OUT} through a 4.7Ω resistor when V_{OUT} is between 5V and 20V to achieve better efficiency. Need to parallel a schottky diode between SW and GND for stability. A SOD-123 package of MBR2100 schottky diode is recommended.

If need a resistor which is larger than 0Ω to limit external mosfet's gate speed, a parallel schottky diode is necessary. Refer to section "Typical Application Circuits".

Internal LDO and BIAS

Most of the internal circuitry is powered by a 5V output internal LDO. This LDO bears voltage from V_{IN} to 5V. When V_{IN} exceeds 5V, the LDO maintain 5V output. When V_{IN} falls below 5V, the output decreases following VIN. For better efficiency and thermal performance, connect BIAS to V_{OUT} through a 4.7Ω resistor, V_{OUT} should between 5V and 20V. In this case the BIAS pin will supply the LSG to drive external LS-FET to improve the efficiency and reduce LDO dissipation. Connect BIAS pin to GND if not use.

■ FUNCTION DESCRIPTIONS (Cont.)

Switching Frequency and External Clock Synchronization

The RT/SYNC PIN can determine the switching frequency and working mode. When set up Non-Sync buck, need to connect the schottky diode between SW and GND. When LSG pin is used, need to connect the external N-MOSFET as the Buck converter LS-FET.

Table 1 Switching frequency set resistor selection

RT/SYNC PIN	Topology/Mode	Switching Frequency
RT/SYNC Short to GND	Non-Sync Buck	2200kHz
$R_{RT/SYNC}$ = 91kΩ		1200kHz
$R_{RT/SYNC}$ = 180kΩ		500kHz
$R_{RT/SYNC}$ = 430kΩ		250kHz
$R_{RT/SYNC}$ = 820kΩ	Sync Buck FPWM Mode	1200kHz
$R_{RT/SYNC}$ = 1.8kΩ		500kHz
RT/SYNC Pin Float		250kHz

The RT/SYNC terminal can receive a frequency synchronization signal from an external system clock. The square wave applied to the RT/SYNC terminal must switch lower than 0.5V and higher than 2V and have a pulse width greater than 20ns. The synchronization frequency range is 200 kHz to 1200kHz. During the transition from the external synchronization mode to the resistor programmed mode, the switching frequency will fall to 250kHz and then increase or decrease to the resistor programmed frequency when the 0.5V bias voltage is reapplied to the RT/SYNC resistor.

Under-Voltage Lockout (UVLO) and Enable (EN) Control

The **UD65501** is enabled when the V_{IN} terminal voltage rises above 4.3V and the EN terminal voltage exceeds the enable threshold of 1.2V. The **UD65501** is disabled when the V_{IN} terminal voltage falls below 4V or when the EN terminal voltage is below 1.2V. The EN terminal has an internal pull-up current source, $I_{EN\_PULL\_UP}$, of 1.2μA that enables operation of the **UD65501** when the EN terminal floats.

For the application which requires a higher under voltage lockout (UVLO) threshold, use the circuit shown below to adjust the input voltage UVLO with two external resistors. When the EN terminal voltage exceeds 1.2V, an additional 3.8μA of hysteresis current, IEN_HYS, is sourced out of the EN terminal. When the EN terminal is pulled below 1.2V, the 3.8μA I_{EN_HYS} current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use below equation to calculate R_{UVLO1} for the desired UVLO hysteresis voltage and R_{UVLO2} for the desired VIN start voltage Enable (EN) is a digital control pin that turns the regulator on and off. Refer below for the calculation formula:

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{EN\_HYS}} \quad (2)$$

$$R_{UVLO2} = \frac{1.2V}{\frac{V_{START} - 1.2V}{R_{UVLO1}} + I_{EN\_PULL\_UP}} \quad (3)$$

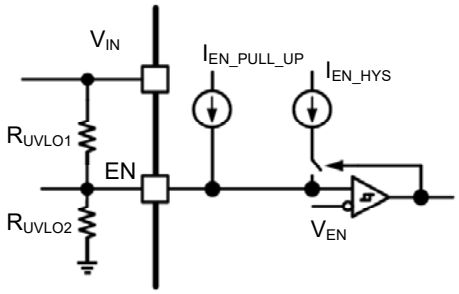


Figure 3. Adjust the Under Voltage Lockout

■ FUNCTION DESCRIPTIONS (Cont.)

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set to 1.2ms internally.

High Duty Mode Operation

UD65501 will automatically extend the on time to support the application when V_{IN} is close to V_{OUT}. The on time extend circuit will be triggered when TOFF-MIN time is reached. The **UD65501** can support up to 99.5% maximum duty cycle.

Current limit and Short protection

The **UD65501** has a peak current limit. During HS-FET on, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after blanking time, the HS-FET would be turn off. The maximum current of the HS-FET is limited cycle-by-cycle internally. Besides, when the output is short, **UD65501** will auto fold back the switching frequency to prevent the current from runaway, to make system reliable.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 140°C), the chip is enabled again.

■ APPLICATION INFORMATION

The **UD65501** output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.803V. The feedback network is shown below Figure.

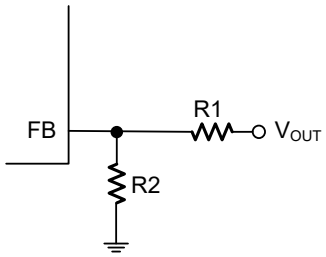


Figure 4. Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2} \quad (4)$$

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from Equation:

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times f_{SW}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L\_MAX}=I_{LOAD}+\frac{\Delta I_L}{2} \quad (6)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 2. Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff} (pF)	L (μH)	C_{OUT} (μF)
12	28	2	33 (Optional)	10	66
5	10.5	2	100 (Optional)	10	66

Note: For a detailed design circuit, please refer to the Typical Application Circuits.

Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_{SW}\times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The **UD65501** can be optimized for a wide range of capacitance and ESR values.

■ APPLICATION INFORMATION (Cont.)

Selecting LS-FET

If use **UD65501** as Sync buck, a N-MOSFET which Qg is less than 20nC with 1.4V to 2.5V $V_{GS(TH)}$ is recommended to achieve better efficiency. There are some MOSFET recommendation.

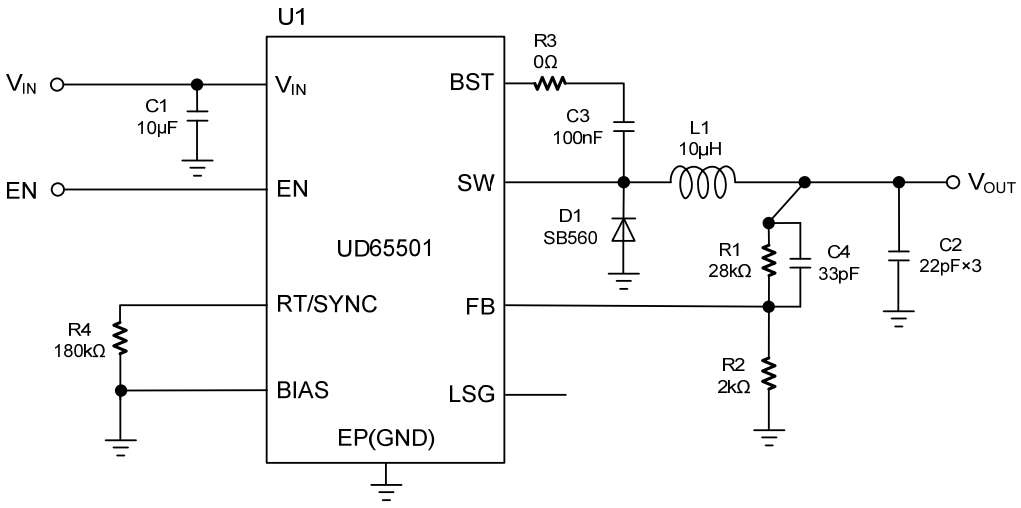
Table 3. LS-FET Recommendation

Manufacturer	Part Number	V_{DS}	I_D	$R_{DS(ON)}$	Q_g	$V_{GS(TH)}$
WINSEMI	SEG9599AG	100V	23A	19.5mΩ (V_{GS}=10V)	22.7nC (V_{GS}=10V)	1.8V
MCC	MCAC38N10YHE3	100V	38A	15mΩ (V_{GS}=10V)	16nC (V_{GS}=10V)	1.8V
APM	APG40N10S	100V	40A	19mΩ (V_{GS}=10V)	16.2nC (V_{GS}=10V)	1.5V

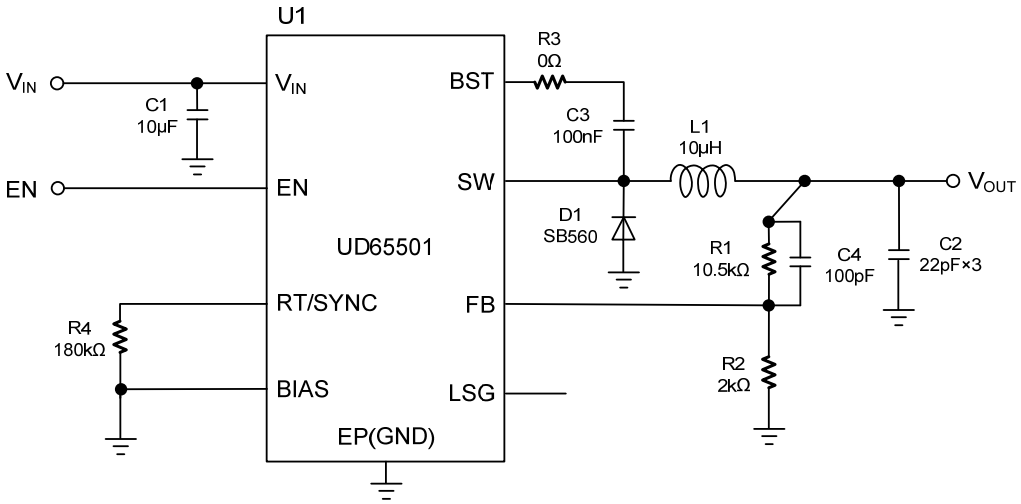
Note: All the parameter is typical value.

■ TYPICAL APPLICATION CIRCUIT

V_{IN}=48V, V_{OUT}=12V/5A, Non-Sync buck, F_{SW}=500kHz

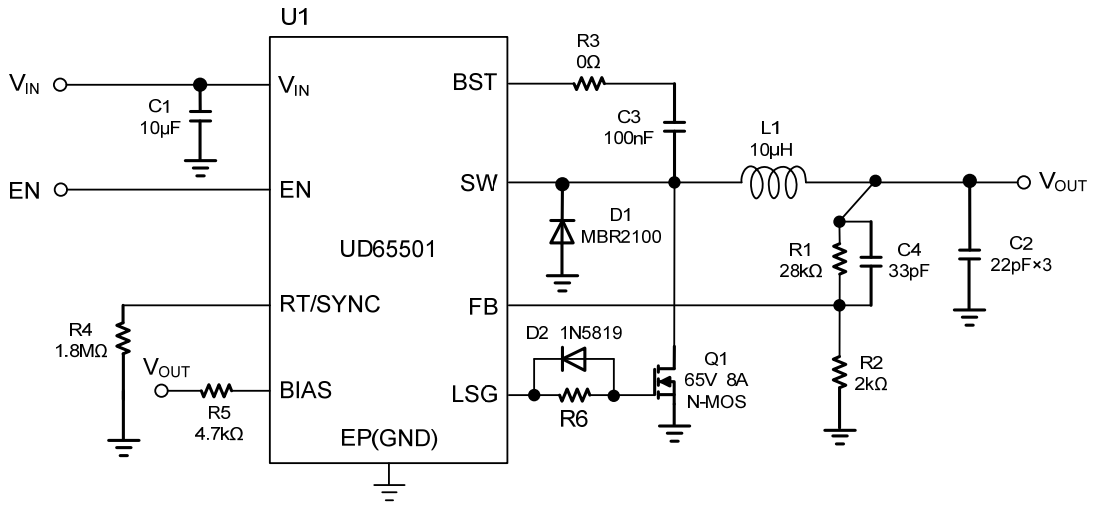


V_{IN}=48V, V_{OUT}=5V/5A, Non-Sync buck, F_{SW}=500kHz



■ TYPICAL APPLICATION CIRCUIT (Cont.)

V_{IN}=48V, V_{OUT}=12V/5A, Sync buck, F_{SW}=500kHz



V_{IN}=48V, V_{OUT}=5V/5A, Sync buck, F_{SW}=500kHz