



USG10R800DMZ

Preliminary

Power MOSFET

N-CHANNEL SGT ENHANCEMENT POWER MOSFET

■ DESCRIPTION

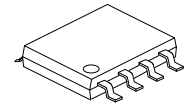
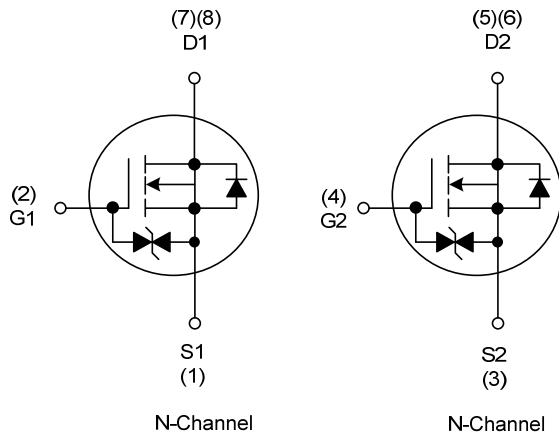
The UTC **USG10R800DMZ** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with high switching speed and low gate charge, etc.

The UTC **USG10R800DMZ** applies to primary side switch, synchronous rectifier, Motor Drives, etc.

■ FEATURES

- * $R_{DS(ON)} \leq 80 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$
 $R_{DS(ON)} \leq 115 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=2.0\text{A}$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

■ SYMBOL



SOP-8

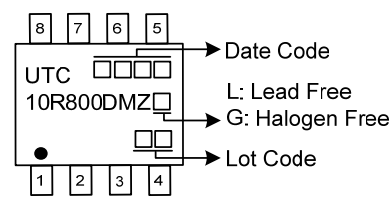
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
USG10R800DMZL-S08-R	USG10R800DMZG-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

USG10R800DMZG-S08-R	
(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) S08: SOP-8
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	8	A
	Pulsed (Note 2)	I_{DM}	16	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	1.8	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.1	V/ns
Power Dissipation		P_D	1.6	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 0.6\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 12\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J \leq T_{JMAX}$, $T_J = 25^{\circ}\text{C}$.

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	125	$^{\circ}\text{C}/\text{W}$
Junction to Case		θ_{JC}	78.1	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

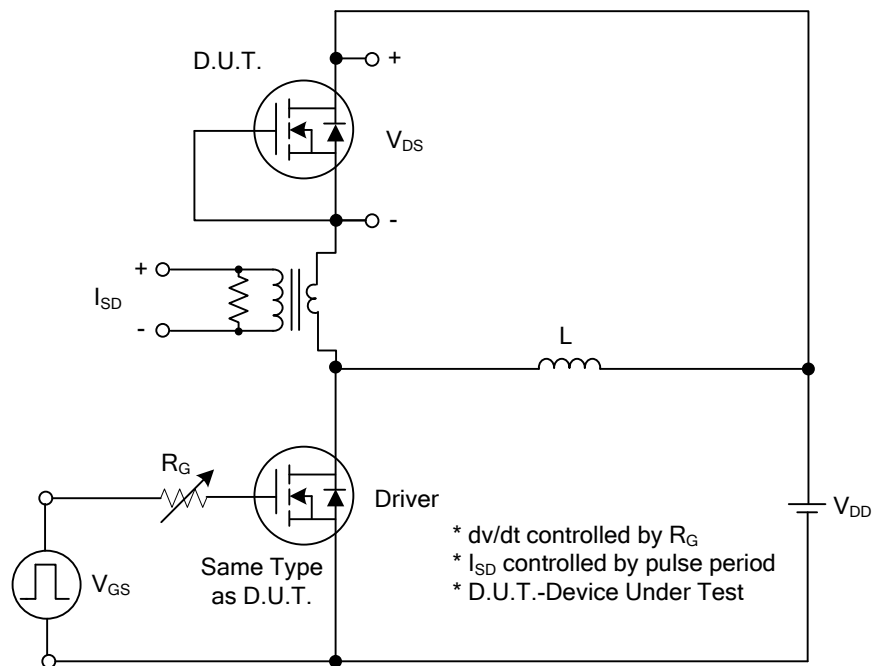
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+10	μA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =4.0A			80	mΩ
			V _{GS} =4.5V, I _D =2.0A			115	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		280		pF
Output Capacitance		C _{OSS}			120		pF
Reverse Transfer Capacitance		C _{RSS}			23		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =80V, V _{GS} =10V, I _D =6A		11		nC
Gate to Source Charge		Q _{GS}			3		nC
Gate to Drain Charge		Q _{GD}			2		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =50V, V _{GS} =10V, I _D =12A, R _G =3Ω		3		ns
Rise Time		t _R			17		ns
Turn-OFF Delay Time		t _{D(OFF)}			10		ns
Fall-Time		t _F			17		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				8	A
Maximum Body-Diode Pulsed Current		I _{SM}				16	A
Drain-Source Diode Forward Voltage		V _{SD}	I _{SD} =12A			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =12A, dI/dt=100A/μs		31		ns
Body Diode Reverse Recovery Charge		Q _{rr}			32		nC

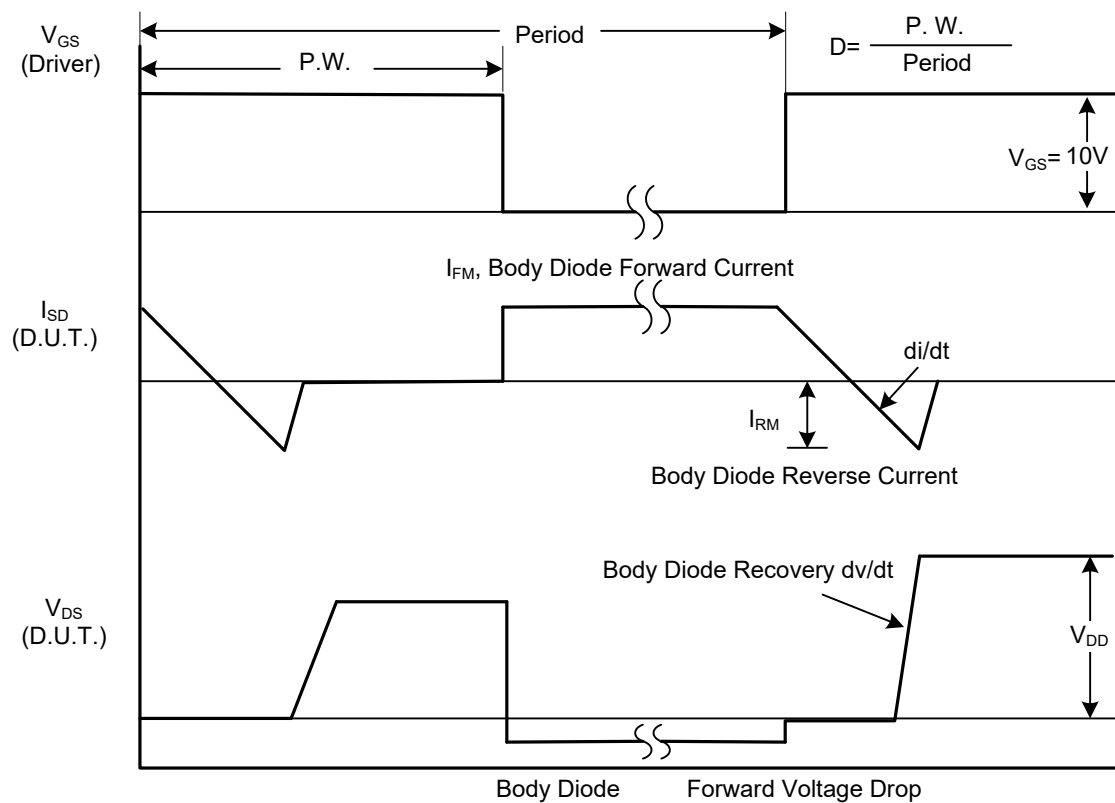
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

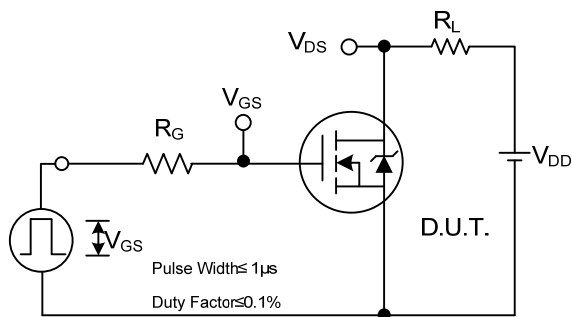


Peak Diode Recovery dv/dt Test Circuit

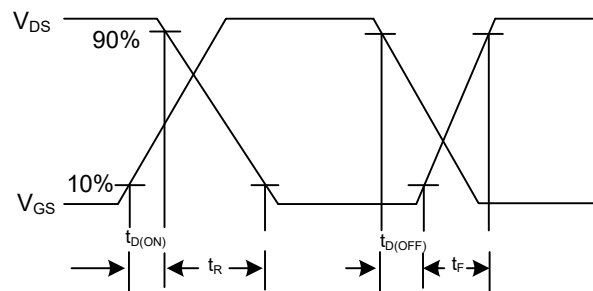


Peak Diode Recovery dv/dt Waveforms

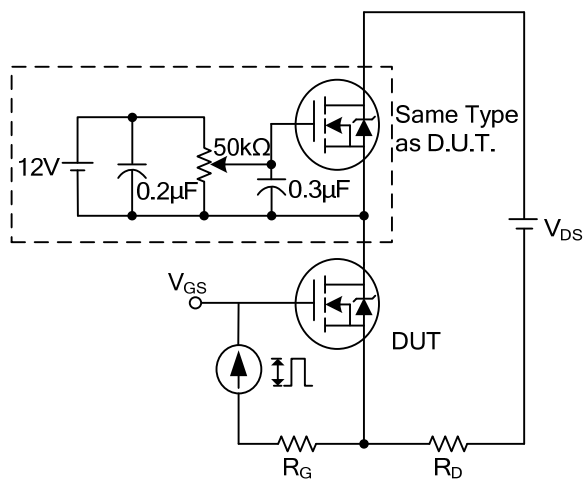
■ TEST CIRCUITS AND WAVEFORMS



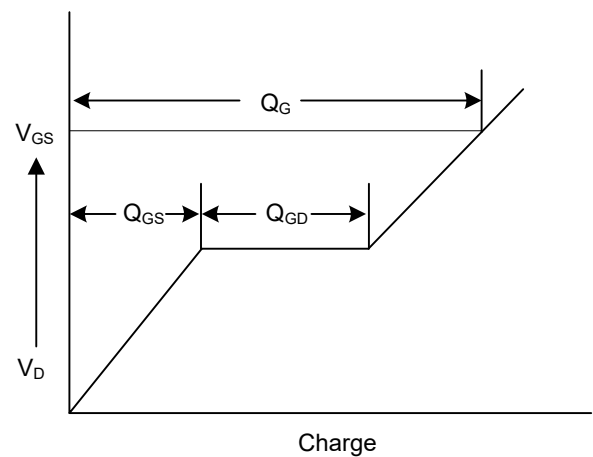
Switching Test Circuit



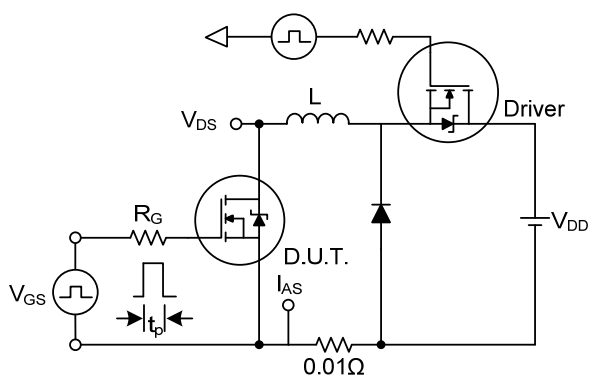
Switching Waveforms



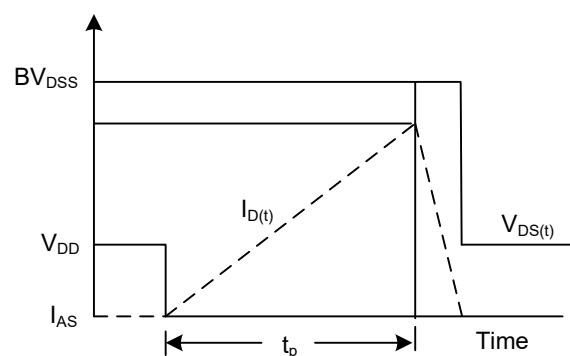
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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