



UT4446B

Power MOSFET

15A, 30V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **UT4446B** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

The UTC **UT4446B** is generally applied in low power switching mode power appliances and electronic ballast.

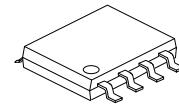
FEATURES

* $R_{DS(ON)} \leq 7.8 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=12\text{A}$

$R_{DS(ON)} \leq 13 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=9.0\text{A}$

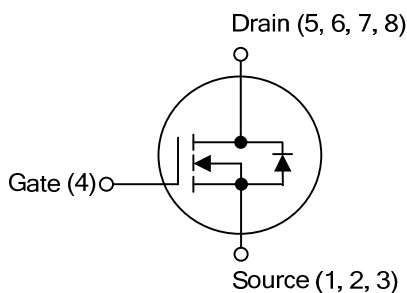
* High Switching Speed

* Improved dv/dt capability



SOP-8

SYMBOL



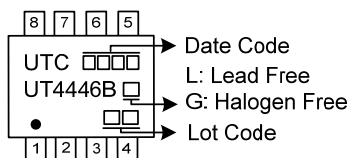
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT4446BL-S08-R	UT4446BG-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT4446BG-S08-R	
(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) S08: SOP-8
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current		I_D	15	A
Pulsed Drain Current (Note 2)		I_{DM}	40	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	4.7	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.7	V/ns
Power Dissipation		P_D	1.9	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Operation and Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 9.7\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 15\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	125	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

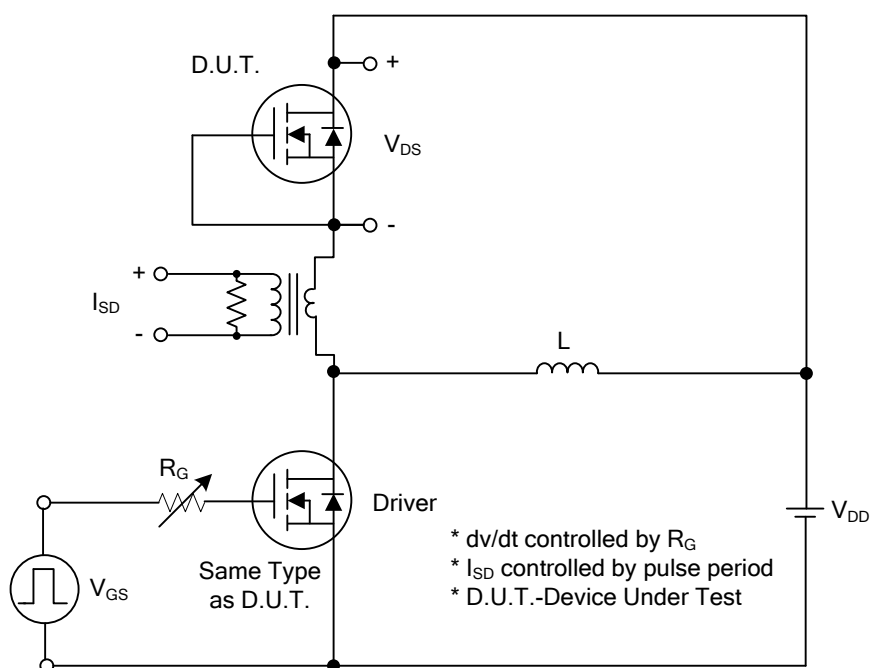
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance (Note 2)		R _{DS(ON)}	V _{GS} =10V, I _D =12A		5.8	7.8	mΩ
			V _{GS} =4.5V, I _D =9.0A		9.0	13	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =15V, f=1.0MHz		972		pF
Output Capacitance		C _{OSS}			258		pF
Reverse Transfer Capacitance		C _{RSS}			220		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q _G	V _{DS} =24V, V _{GS} =10V, I _D =15A		44		nC
Gate to Source Charge		Q _{GS}			5		nC
Gate to Drain Charge		Q _{GD}			14		nC
Turn-ON Delay Time (Note 2)		t _{D(ON)}	V _{DS} =15V, V _{GS} =10V, I _D =15A, R _G =3.3Ω		8		ns
Rise Time		t _R			18		ns
Turn-OFF Delay Time		t _{D(OFF)}			28		ns
Fall-Time		t _F			23		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				15	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				40	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =15A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =15A, V _{GS} =0V,		287		nS
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		797		nC

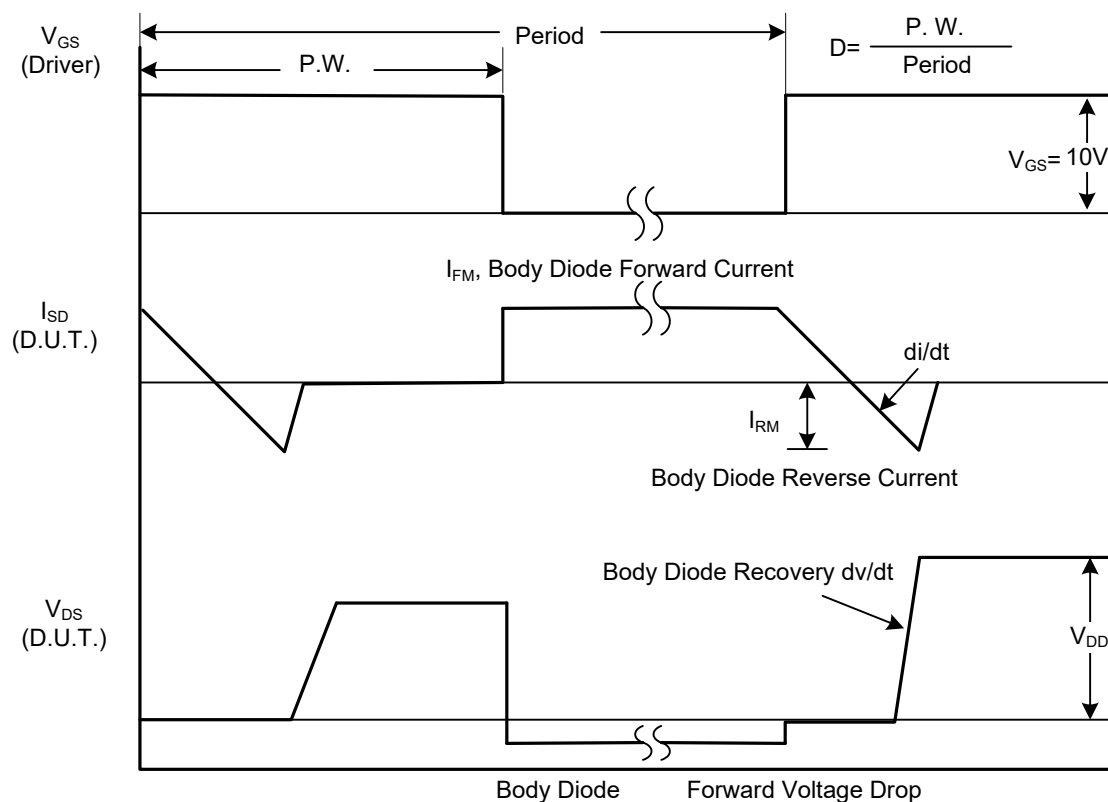
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS

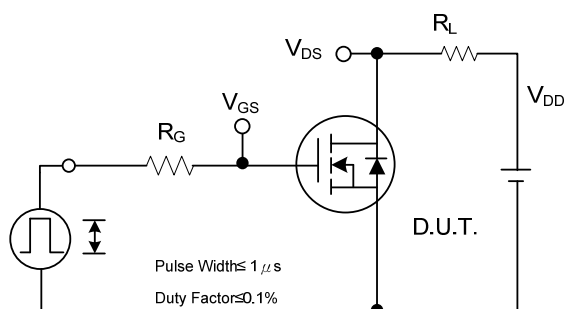


Fig. 2A Switching Test Circuit

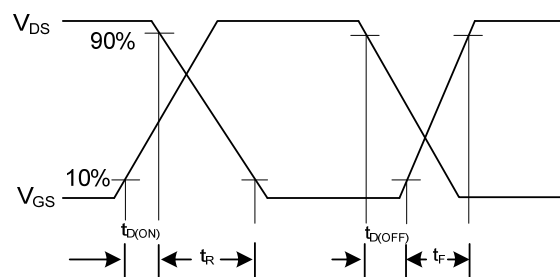


Fig. 2B Switching Waveforms

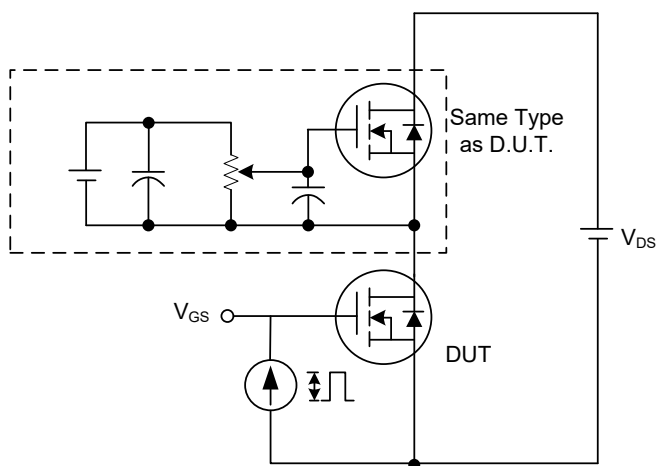


Fig. 3A Gate Charge Test Circuit

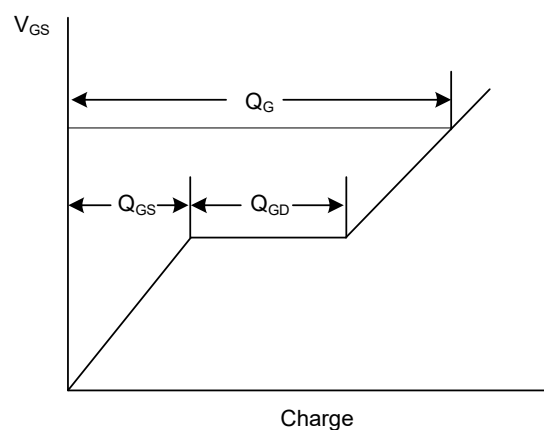


Fig. 3B Gate Charge Waveform

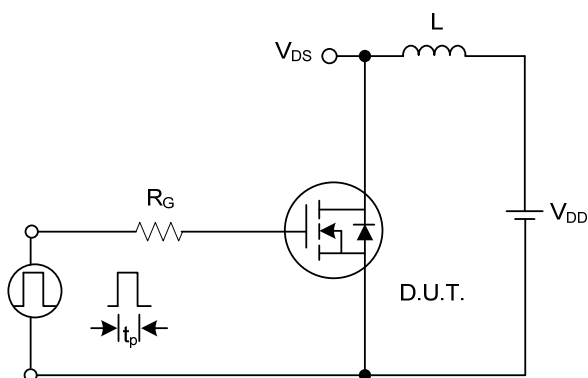


Fig. 4A Unclamped Inductive Switching Test Circuit

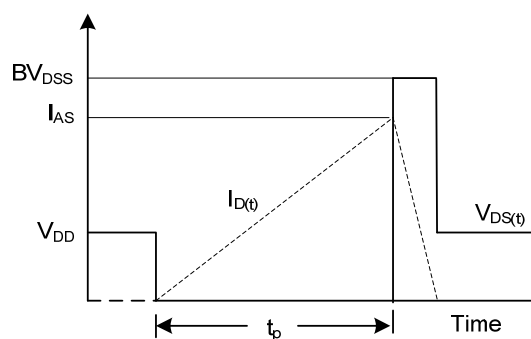
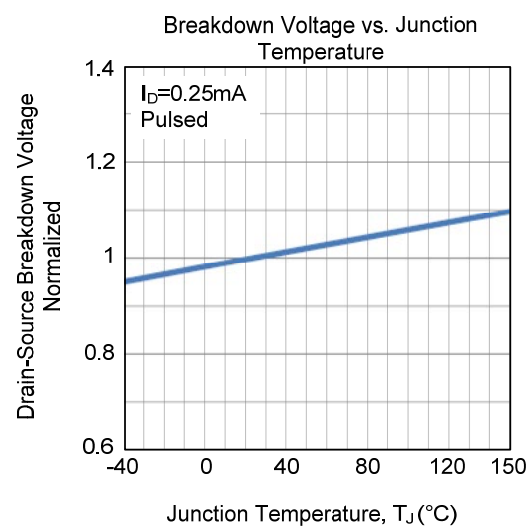
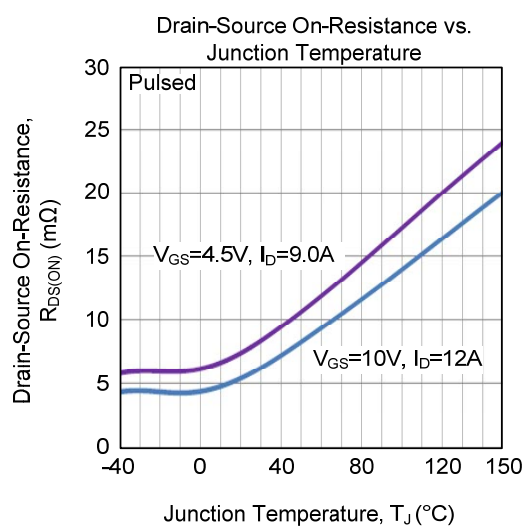
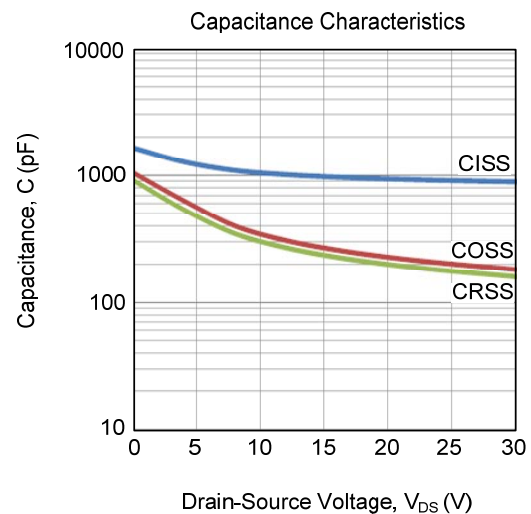
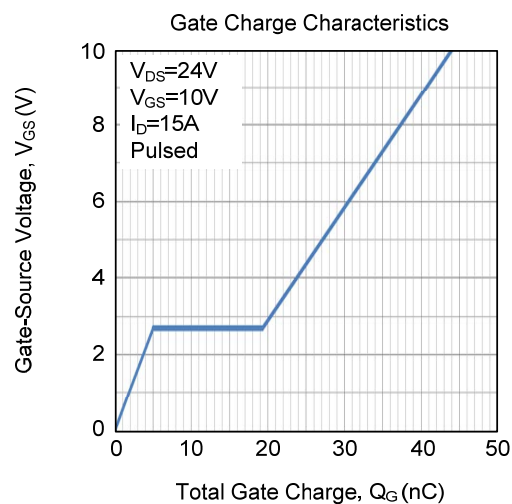
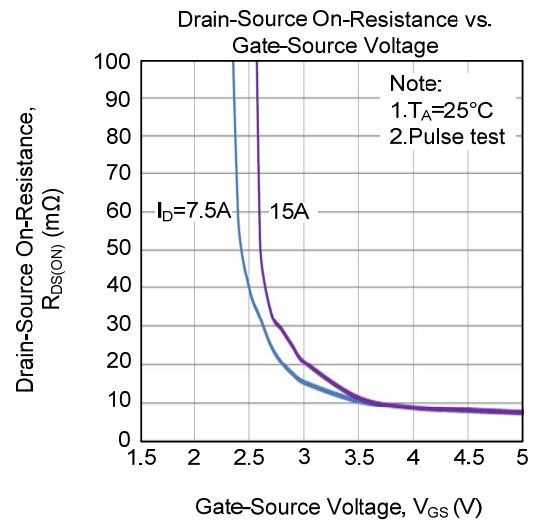
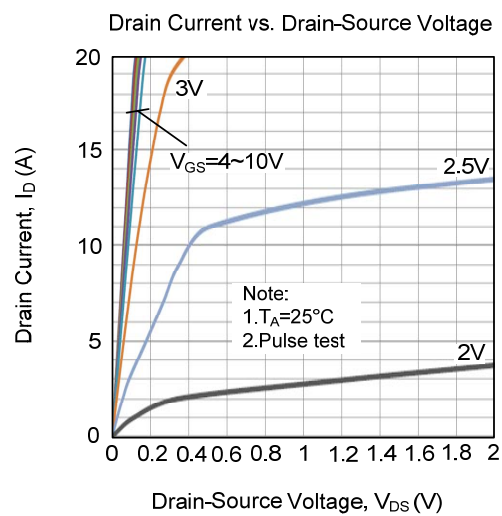
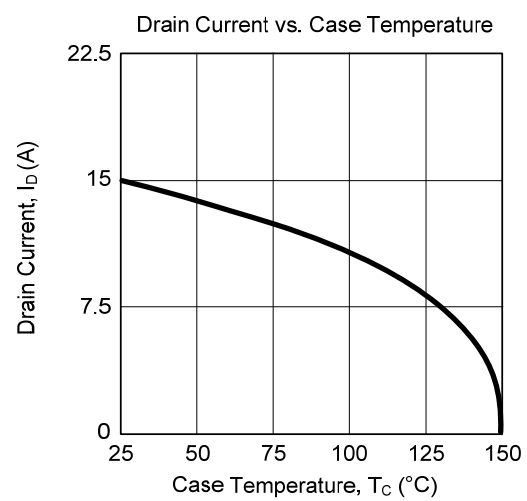
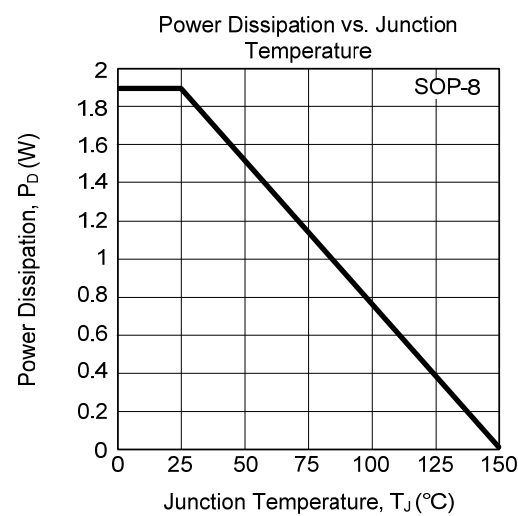
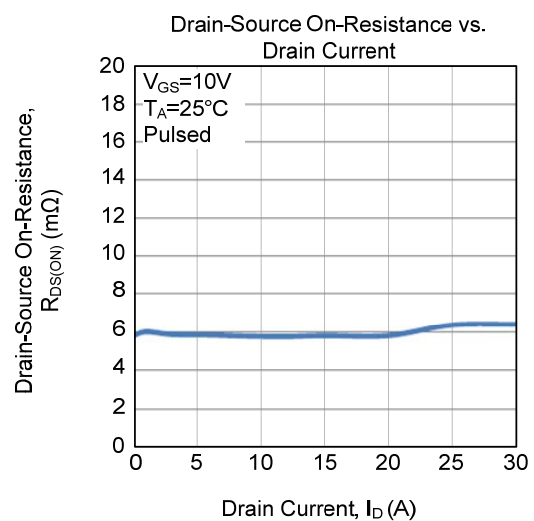
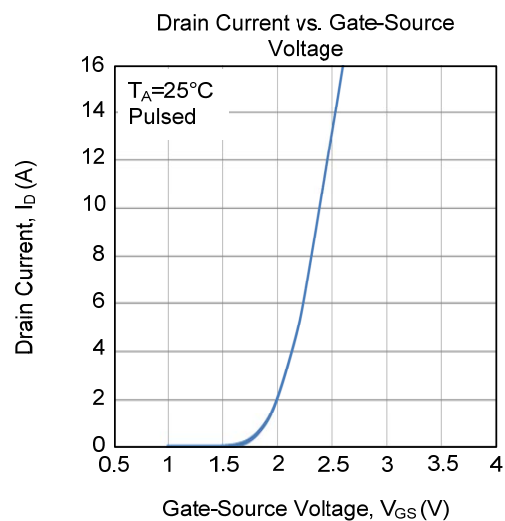
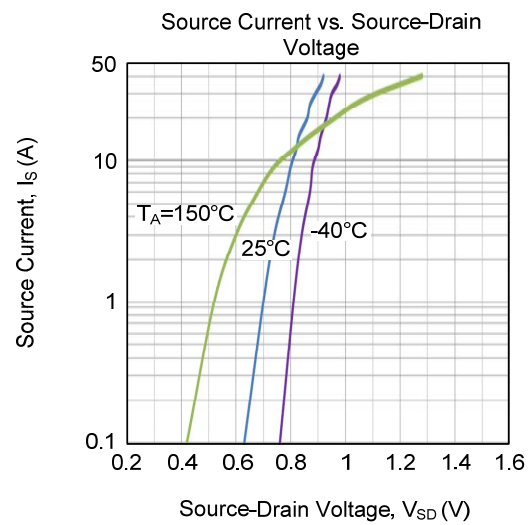
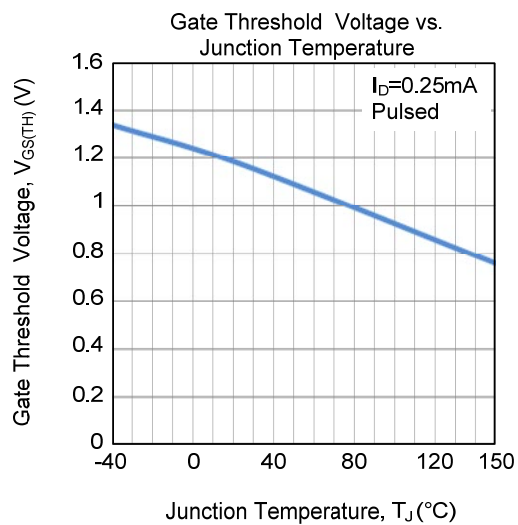


Fig. 4B Unclamped Inductive Switching Waveforms

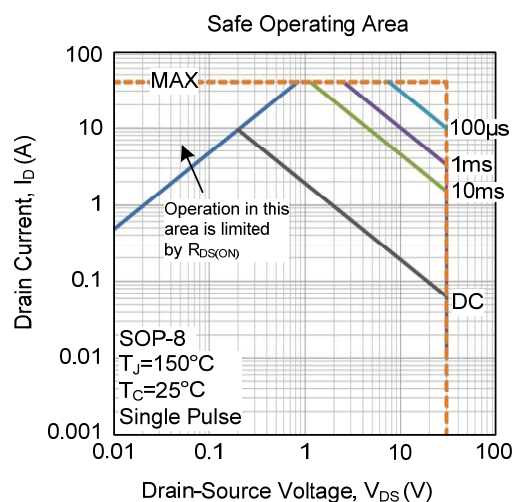
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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