



UT50N06H

Preliminary

POWER MOSFET

**50A, 60V N-CHANNEL
POWER MOSFET**

■ DESCRIPTION

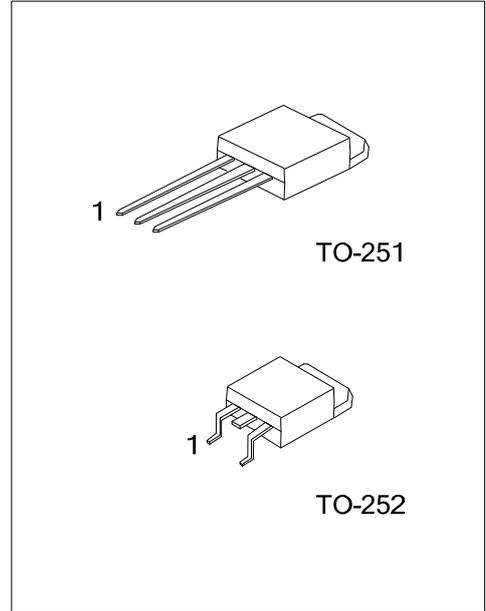
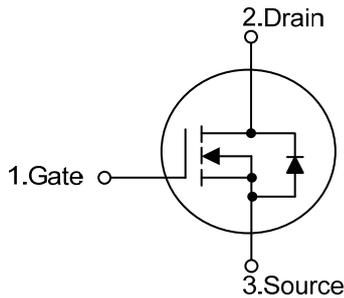
The UTC **UT50N06H** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance, low gate charge and high switching speed.

The UTC **UT50N06H** is suitable for high voltage synchronous rectifier and DC/DC converters, etc.

■ FEATURES

- * $R_{DS(ON)} \leq 16 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=25\text{A}$
- * High Switching Speed
- * High Cell Density Trench Technology

■ SYMBOL



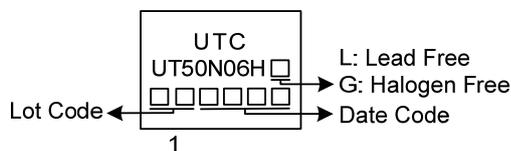
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT50N06HL-TM3-T	UT50N06HG-TM3-T	TO-251	G	D	S	Tube
UT50N06HL-TN3-R	UT50N06HG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT50N06HG-TM3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TM3: TO-251, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	50	A
	Pulsed (Note 2)	I_{DM}	100	A
Avalanche Energy (Note 3)	Single Pulsed (Note 3)	E_{AS}	32	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	18.1	V/ns
Power Dissipation		P_D	51	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-50 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 0.1\text{mH}$, $I_{AS} = 25.4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.45 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

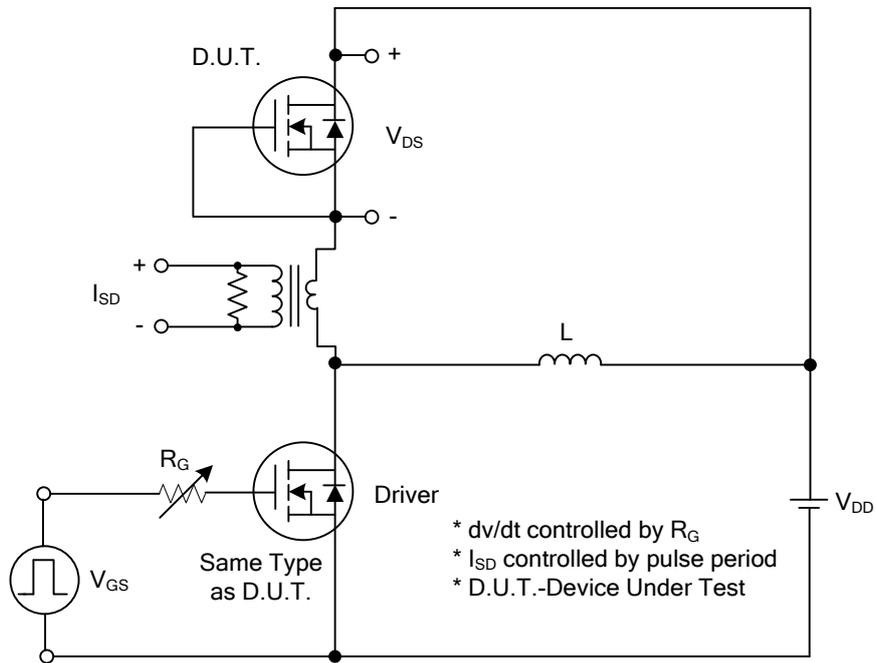
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	60			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	Forward $V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
		Reverse $V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=25\text{A}$			16	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		1537		pF
Output Capacitance	C_{OSS}			170		pF
Reverse Transfer Capacitance	C_{RSS}			142		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=48\text{V}$, $V_{GS}=10\text{V}$, $I_D=50\text{A}$ (Note 1, 2)		51		nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain Charge	Q_{GD}			24		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=50\text{A}$, $R_G=3\Omega$ (Note 1, 2)		10		ns
Rise Time	t_R			18		ns
Turn-off Delay Time	$t_{D(OFF)}$			26		ns
Fall-Time	t_F			19		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				50	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=50\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=30\text{A}$, $V_{GS}=0\text{V}$, $di_F/dt=100\text{A}/\mu\text{s}$		34		ns
Body Diode Reverse Recovery Charge	Q_{rr}				28	

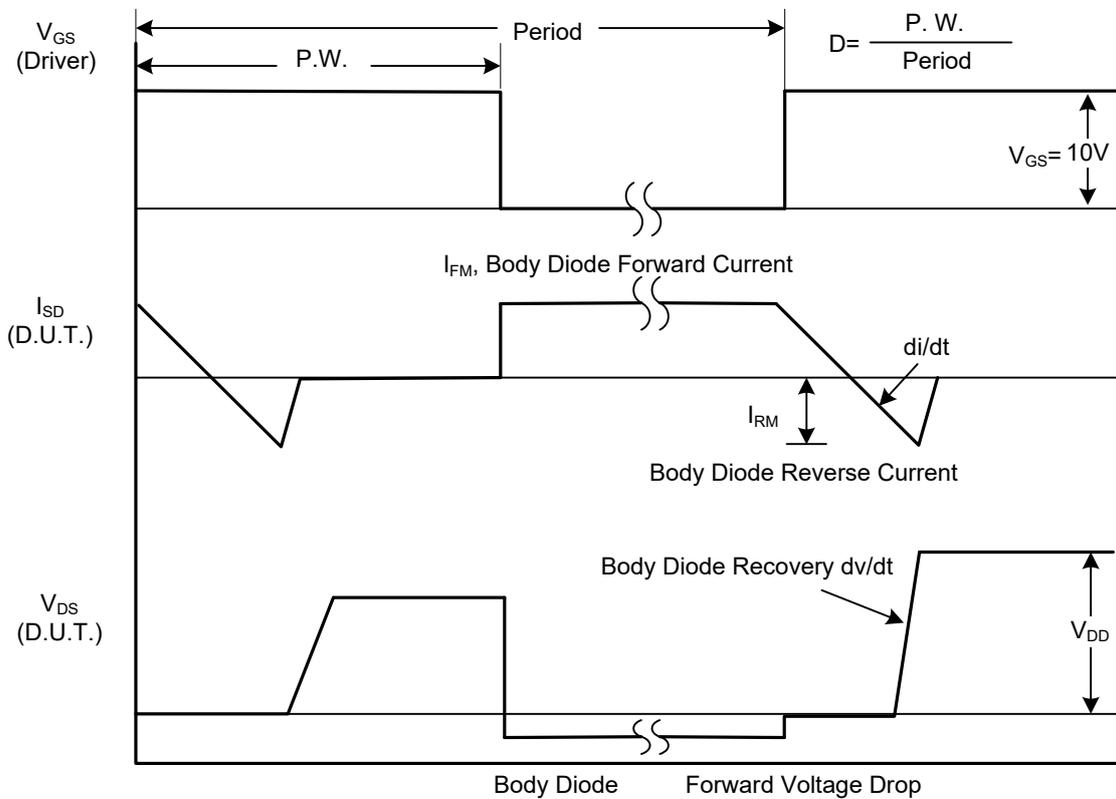
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

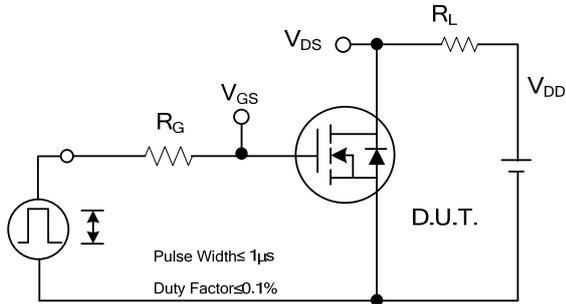


Peak Diode Recovery dv/dt Test Circuit

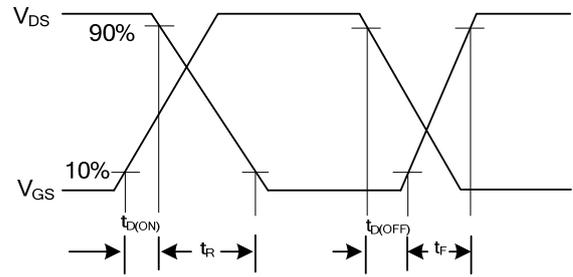


Peak Diode Recovery dv/dt Waveforms

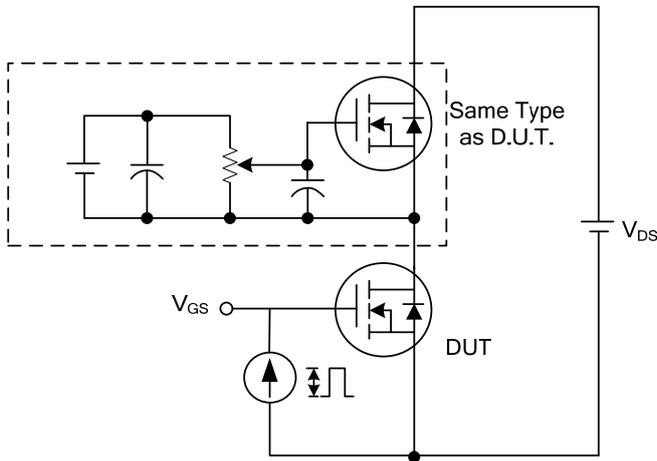
TEST CIRCUITS AND WAVEFORMS



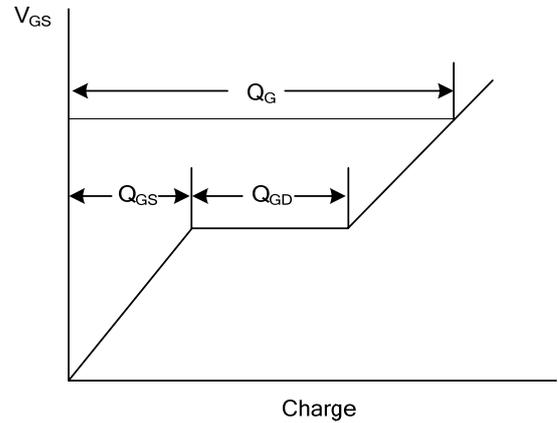
Switching Test Circuit



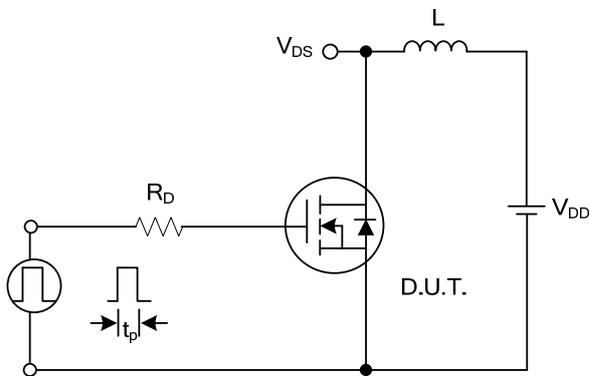
Switching Waveforms



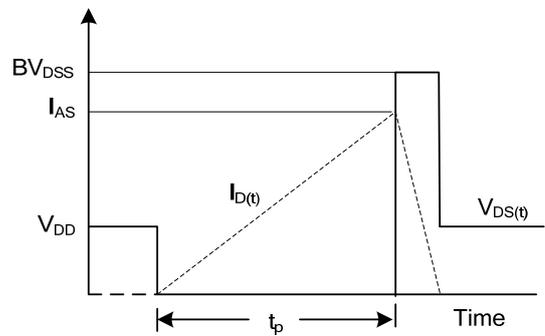
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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