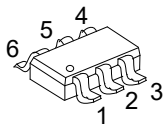
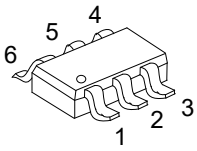
U74AVC1T45B **Preliminary** ***CMOS IC***

SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



SOT-363



SOT-26

■ DESCRIPTION

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The UTC **U74AVC1T45B** is optimized to operate with V_{CCA}/V_{CCB} set at 1.4V to 3.6V. It is operational with V_{CCA}/V_{CCB} as low as 0.8V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 0.8V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 0.8V to 3.6V. This allows for universal low-Voltage, bidirectional translation between any of the 0.8V, 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

■ FEATURES

* V_{CC} Isolation Feature: If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
* Dual Supply Rail Design
* DIR Input Circuit Referenced to V_{CCA}
* ±12mA Output Drive at 3.3V
* I/Os Are 4.6V Over Voltage Tolerant
* I_{OFF} Supports Partial-Power-Down Mode Operation

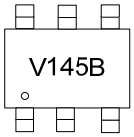
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AVC1T45BL-AG6-R	U74AVC1T45BG-AG6-R	SOT-26	Tape Reel
U74AVC1T45BL-AL6-R	U74AVC1T45BG-AL6-R	SOT-363	Tape Reel

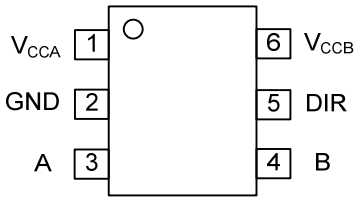
U74AVC1T45BG-AG6-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) AG6: SOT-26, AL6: SOT-363
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



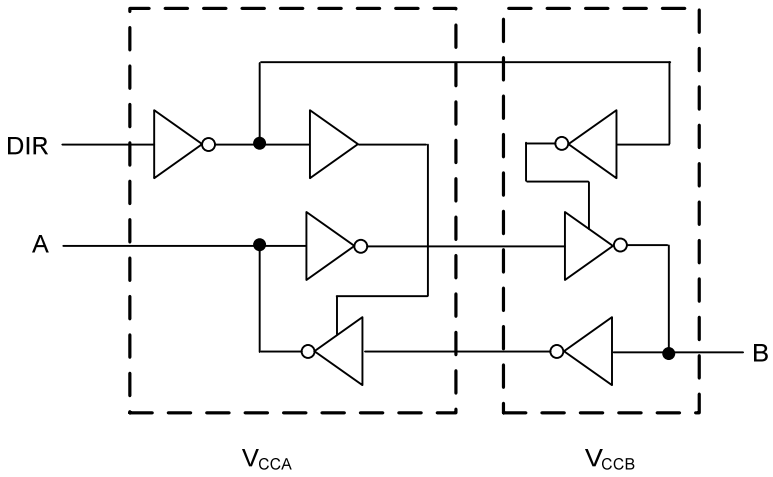
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	V_{CCA}	P	A-port supply voltage. 0.8V ≤ V_{CCA} ≤ 3.6V
2	GND	G	Ground
3	A	I/O	Input/output A. Referenced to V_{CCA}
4	B	I/O	Input/output B. Referenced to V_{CCB}
5	DIR	I	Direction control signal
6	V_{CCB}	P	B-port supply voltage. 0.8V ≤ V_{CCB} ≤ 3.6V

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CCA}		-0.5 ~ 4.6	V
Supply Voltage	V_{CCB}		-0.5 ~ 4.6	V
Input Voltage (Note 2)	V_{IN}	I/O ports (A port)	-0.5 ~ 4.6	V
		I/O ports (B port)	-0.5 ~ 4.6	V
		Control Inputs	-0.5 ~ 4.6	V
Voltage Applied to any Output in the High-Impedance or Power Off State (Note 2)	V_{OUT}	A Port	-0.5 ~ 4.6	V
		B Port	-0.5 ~ 4.6	V
Voltage applied to any output in the high or low state (Note 2, 3)	V_{OUT}	A Port	-0.5 ~ V_{CCA}+0.5	V
		B Port	-0.5 ~ V_{CCB}+0.5	V
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0V	-50	mA
Continuous Output Current	I_{OUT}		±50	mA
Continuous current through V_{CCA}, V_{CCB} or GND			±100	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CCA}		0.8		3.6	V
Supply Voltage		V_{CCB}		0.8		3.6	V
High-Level Input Voltage	Data Inputs	V_{IH}	V_{CCI}=0.8V	V_{CCI} ×0.8			V
			V_{CCI}=1.2~1.95V	V_{CCI} ×0.65			V
			V_{CCI}=1.95V~2.7V	1.6			V
			V_{CCI}=2.7V~3.6V	2			V
	DIR (Referenced to V_{CCA})		V_{CCI}=0.8V	V_{CCA} ×0.7			V
			V_{CCI}=1.2V~1.95V	V_{CCA} ×0.65			V
			V_{CCI}=1.95V~2.7V	1.6			V
			V_{CCI}=2.7V~3.6V	2.3			V
Low-Level Input Voltage	Data Inputs	V_{IL}	V_{CCI}=0.8V			V_{CCI} ×0.2	V
			V_{CCI}=1.2V~1.95V			V_{CCI} ×0.35	V
			V_{CCI}=1.95V~2.7V			0.7	V
			V_{CCI}=2.7V~3.6V			0.8	V
	DIR (Referenced to V_{CCA})		V_{CCI}=0.8V			V_{CCA} ×0.3	V
			V_{CCI}=1.2V~1.95V			V_{CCA} ×0.35	V
			V_{CCI}=1.95V~2.7V			0.7	V
			V_{CCI}=2.7V~3.6V			0.8	V
Input Voltage		V_{IN}		0		3.6	V
Output Voltage	Active State	V_{OUT}		0		V_{CCO}	V
	3-State			0		3.6	V
Input Transition Rise or Fall Rate		Δt/Δv				5	ns/V
Operating Temperature		T_A		-40		+85	°C

Notes: 1. V_{CCI} is the V_{CC} associated with the input port.
2. V_{CCO} is the V_{CC} associated with the output port.
3. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	230	°C/W
Junction to Case	θ_{JC}	90	°C/W

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+85°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Output Voltage	V_{OH}	V_I=V_{IH}	V_{CCA}=0.8V~3.6V V_{CCB}=0.8V~3.6V I_{OH}=-100μA	V_{CCO} -0.2			V_{CCO} -0.2			V
			V_{CCA}=1.2V, V_{CCB}=1.2V I_{OH}=-3mA	0.85			0.85			V
			V_{CCA}=1.4V, V_{CCB}=1.4V I_{OH}=-6mA	1.05			1.05			V
			V_{CCA}=1.65V, V_{CCB}=1.65V I_{OH}=-8mA	1.2			1.2			V
			V_{CCA}=2.3V, V_{CCB}=2.3V I_{OL}=-9mA	1.75			1.75			V
			V_{CCA}=3V, V_{CCB}=3V I_{OL}=12mA	2.3			2.3			V
Low-Level Output Voltage	V_{OL}	V_I=V_{IL}	V_{CCA}=0.8V~3.6V V_{CCB}=0.8V~3.6V I_{OL}=100μA			0.2			0.2	V
			V_{CCA}=1.2V, V_{CCB}=1.2V I_{OL}=3mA			0.25			0.25	V
			V_{CCA}=1.4V, V_{CCB}=1.4V I_{OL}=6mA			0.35			0.35	V
			V_{CCA}=1.65V, V_{CCB}=1.65V I_{OL}=8mA			0.45			0.45	V
			V_{CCA}=2.3V, V_{CCB}=2.3V I_{OL}=9mA			0.55			0.55	V
			V_{CCA}=3V, V_{CCB}=3V I_{OL}=12mA			0.7			0.7	V

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+85°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Input Leakage Current	DIR	I_I	V_I=V_{CCA} or GND, V_{CCA}=0.8V~3.6V, V_{CCB}=0.8V~3.6V		-0.25		0.25	-1		1	μA
Power OFF Leakage Current	A Port	I_{OFF}	V_{IN} or V_{OUT}=0~3.6V, V_{CCA}=0V, V_{CCB}=0V~3.6V		-1		1	-5		5	μA
	B Port		V_{IN} or V_{OUT}=0~3.6V, V_{CCA}=0V~3.6V, V_{CCB}=0V		-1		1	-5		5	μA
Output OFF-State Current	A Port	I_{OZ}	V_{OUT}=V_{CCO} or GND, V_{IN}=V_{CCI} or GND, V_{CCA}=0V, V_{CCB}=3.6V		-2.5		2.5	-5		5	μA
	B Port		V_{OUT}=V_{CCO} or GND, V_{IN}=V_{CCI} or GND, V_{CCA}=3.6V, V_{CCB}=0V		-2.5		2.5	-5		5	μA
Supply A Current		I_{CCA}	V_{IN}=V_{CCI} or GND, I_{OUT}=0A	V_{CCA}=0.8V~3.6V V_{CCB}=0.8V~3.6V			10			12	μA
				V_{CCA}=0V, V_{CCB}=3.6V			-2			-8	μA
				V_{CCA}=3.6V, V_{CCB}=0V			10			12	μA
Supply B Current		I_{CCB}	V_{IN}=V_{CCI} or GND, I_{OUT}=0A	V_{CCA}=0.8V~3.6V, V_{CCB}=0.8V~3.6V			10			12	μA
				V_{CCA}=0V, V_{CCB}=3.6V			10			12	μA
				V_{CCA}=3.6V, V_{CCB}=0V			-2			-8	μA
Supply A Current Plus Supply B Current		I_{CCA}+I_{CCB}	V_{IN}=V_{CCI} or GND, I_{OUT}=0A	V_{CCA}=0.8V~3.6V, V_{CCB}=0.8V~3.6V			20			24	μA

Notes: 1. V_{CCO} is the V_{CC} associated with the output port.
2. V_{CCI} is the V_{CC} associated with the input port.

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A) to Output (B)	t_{PLH} t_{PHL}	V_{CCA}=0.8V	V_{CCB}=0.8V		100		ns
			V_{CCB}=1.2V		88		ns
			V_{CCB}=1.5V		79		ns
			V_{CCB}=1.8V		70		ns
			V_{CCB}=2.5V		49		ns
			V_{CCB}=3.3V		25		ns
Propagation Delay From Input (B) to Output (A)		V_{CCA}=0.8V	V_{CCB}=0.8V		100		ns
			V_{CCB}=1.2V		95		ns
			V_{CCB}=1.5V		91		ns
			V_{CCB}=1.8V		87		ns
			V_{CCB}=2.5V		78		ns
			V_{CCB}=3.3V		70		ns
Propagation Delay From Input (A) to Output (B)		V_{CCB}=0.8V	V_{CCA}=0.8V		100		ns
			V_{CCA}=1.2V		95		ns
			V_{CCA}=1.5V		91		ns
			V_{CCA}=1.8V		87		ns
			V_{CCA}=2.5V		78		ns
			V_{CCA}=3.3V		70		ns
Propagation Delay From Input (B) to Output (A)		V_{CCB}=0.8V	V_{CCA}=0.8V		100		ns
			V_{CCA}=1.2V		88		ns
			V_{CCA}=1.5V		79		ns
			V_{CCA}=1.8V		70		ns
			V_{CCA}=2.5V		49		ns
			V_{CCA}=3.3V		25		ns
Propagation Delay From Input (DIR) to Output (A)	t_{PHZ} t_{PLZ}	V_{CCA}=0.8V	V_{CCB}=0.8V		68		ns
			V_{CCB}=1.2V		68		ns
			V_{CCB}=1.5V		68		ns
			V_{CCB}=1.8V		68		ns
			V_{CCB}=2.5V		68		ns
			V_{CCB}=3.3V		68		ns
Propagation Delay From Input (DIR) to Output (B)		V_{CCA}=0.8V	V_{CCB}=0.8V		65		ns
			V_{CCB}=1.2V		58		ns
			V_{CCB}=1.5V		52		ns
			V_{CCB}=1.8V		46		ns
			V_{CCB}=2.5V		33		ns
			V_{CCB}=3.3V		20		ns
Propagation Delay From Input (DIR) to Output (A)		V_{CCB}=0.8V	V_{CCA}=0.8V		68		ns
			V_{CCA}=1.2V		61		ns
			V_{CCA}=1.5V		55		ns
			V_{CCA}=1.8V		49		ns
			V_{CCA}=2.5V		36		ns
			V_{CCA}=3.3V		23		ns
Propagation Delay From Input (DIR) to Output (B)		V_{CCB}=0.8V	V_{CCA}=0.8V		65		ns
			V_{CCA}=1.2V		60		ns
			V_{CCA}=1.5V		56		ns
			V_{CCA}=1.8V		52		ns
			V_{CCA}=2.5V		44		ns
			V_{CCA}=3.3V		35		ns

■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (DIR) to Output (A)	t_{PZL} t_{PZH}	V_{CCA}=0.8V	V_{CCB}=0.8V		130		ns
			V_{CCB}=1.2V		50		ns
			V_{CCB}=1.5V		25		ns
			V_{CCB}=1.8V		20		ns
			V_{CCB}=2.5V		20		ns
			V_{CCB}=3.3V		20		ns
Propagation Delay From Input (DIR) to Output (B)		V_{CCA}=0.8V	V_{CCB}=0.8V		130		ns
			V_{CCB}=1.2V		118		ns
			V_{CCB}=1.5V		109		ns
			V_{CCB}=1.8V		100		ns
			V_{CCB}=2.5V		79		ns
			V_{CCB}=3.3V		58		ns
Propagation Delay From Input (DIR) to Output (A)		V_{CCB}=0.8V	V_{CCA}=0.8V		130		ns
			V_{CCA}=1.2V		70		ns
			V_{CCA}=1.5V		65		ns
			V_{CCA}=1.8V		65		ns
			V_{CCA}=2.5V		65		ns
			V_{CCA}=3.3V		70		ns
Propagation Delay From Input (DIR) to Output (B)		V_{CCB}=0.8V	V_{CCA}=0.8V		130		ns
			V_{CCA}=1.2V		110		ns
			V_{CCA}=1.5V		95		ns
			V_{CCA}=1.8V		80		ns
			V_{CCA}=2.5V		45		ns
			V_{CCA}=3.3V		10		ns

■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+85°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input (A) to Output (B)	t_{PLH} t_{PHL}	V_{CCA}=1.2V±0.1V	V_{CCB}=1.2V±0.1V	0.1		21	0.1		21.9	ns
			V_{CCB}=1.5V±0.1V	0.1		16.8	0.1		17.5	ns
			V_{CCB}=1.8V±0.15V	0.1		14.1	0.1		14.8	ns
			V_{CCB}=2.5V±0.2V	0.1		12.7	0.1		13.3	ns
			V_{CCB}=3.3V±0.3V	0.1		11.1	0.1		11.8	ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V±0.1V	0.1		19	0.1		19.8	ns
			V_{CCB}=1.5V±0.1V	0.1		14.4	0.1		15	ns
			V_{CCB}=1.8V±0.15V	0.1		11.6	0.1		12.1	ns
			V_{CCB}=2.5V±0.2V	0.1		9.7	0.1		10.1	ns
			V_{CCB}=3.3V±0.3V	0.1		7.5	0.1		7.9	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V±0.1V	0.1		17.7	0.1		18.5	ns
			V_{CCB}=1.5V±0.1V	0.1		13.1	0.1		13.7	ns
			V_{CCB}=1.8V±0.15V	0.1		10.3	0.1		10.8	ns
			V_{CCB}=2.5V±0.2V	0.1		8.4	0.1		8.8	ns
			V_{CCB}=3.3V±0.3V	0.1		6.1	0.1		6.5	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V±0.1V	0.1		16.2	0.1		17	ns
			V_{CCB}=1.5V±0.1V	0.1		11.7	0.1		12.2	ns
			V_{CCB}=1.8V±0.15V	0.1		8.9	0.1		9.3	ns
			V_{CCB}=2.5V±0.2V	0.1		7	0.1		7.3	ns
			V_{CCB}=3.3V±0.3V	0.1		4.6	0.1		4.9	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V±0.1V	0.1		16.1	0.1		16.9	ns
			V_{CCB}=1.5V±0.1V	0.1		11.5	0.1		12	ns
			V_{CCB}=1.8V±0.15V	0.1		8.7	0.1		9.1	ns
			V_{CCB}=2.5V±0.2V	0.1		6.8	0.1		7.1	ns
			V_{CCB}=3.3V±0.3V	0.1		4.4	0.1		4.7	ns
Propagation Delay From Input (B) to Output (A)	t_{PLH} t_{PHL}	V_{CCA}=1.2V±0.1V	V_{CCB}=1.2V±0.1V	0.1		21	0.1		21.9	ns
			V_{CCB}=1.5V±0.1V	0.1		18	0.1		18.8	ns
			V_{CCB}=1.8V±0.15V	0.1		15.7	0.1		16.5	ns
			V_{CCB}=2.5V±0.2V	0.1		14.2	0.1		15	ns
			V_{CCB}=3.3V±0.3V	0.1		12.1	0.1		12.9	ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V±0.1V	0.1		17.8	0.1		18.5	ns
			V_{CCB}=1.5V±0.1V	0.1		14.4	0.1		15	ns
			V_{CCB}=1.8V±0.15V	0.1		12.1	0.1		12.7	ns
			V_{CCB}=2.5V±0.2V	0.1		10.7	0.1		11.2	ns
			V_{CCB}=3.3V±0.3V	0.1		8.5	0.1		9	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V±0.1V	0.1		16.1	0.1		16.8	ns
			V_{CCB}=1.5V±0.1V	0.1		12.6	0.1		13.1	ns
			V_{CCB}=1.8V±0.15V	0.1		10.4	0.1		10.9	ns
			V_{CCB}=2.5V±0.2V	0.1		8.9	0.1		9.3	ns
			V_{CCB}=3.3V±0.3V	0.1		6.7	0.1		7.1	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V±0.1V	0.1		14.7	0.1		15.3	ns
			V_{CCB}=1.5V±0.1V	0.1		10.8	0.1		11.2	ns
			V_{CCB}=1.8V±0.15V	0.1		8.4	0.1		8.8	ns
			V_{CCB}=2.5V±0.2V	0.1		7	0.1		7.3	ns
			V_{CCB}=3.3V±0.3V	0.1		4.8	0.1		5.1	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V±0.1V	0.1		15.1	0.1		15.8	ns
			V_{CCB}=1.5V±0.1V	0.1		10.6	0.1		11	ns
			V_{CCB}=1.8V±0.15V	0.1		8.1	0.1		8.5	ns
			V_{CCB}=2.5V±0.2V	0.1		6.6	0.1		6.9	ns
			V_{CCB}=3.3V±0.3V	0.1		4.4	0.1		4.7	ns

■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+85°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input (DIR) to Output (A)	t_{PHZ} t_{PLZ}	V_{CCA}=1.2V±0.1V	V_{CCB}=1.2V±0.1V	0.1		19.8	0.1		20.7	ns
			V_{CCB}=1.5V±0.1V	0.1		19.8	0.1		20.7	ns
			V_{CCB}=1.8V±0.15V	0.1		19.8	0.1		20.7	ns
			V_{CCB}=2.5V±0.2V	0.1		19.8	0.1		20.7	ns
			V_{CCB}=3.3V±0.3V	0.1		19.8	0.1		20.7	ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V±0.1V	0.1		15.3	0.1		16	ns
			V_{CCB}=1.5V±0.1V	0.1		15.3	0.1		16	ns
			V_{CCB}=1.8V±0.15V	0.1		15.3	0.1		16	ns
			V_{CCB}=2.5V±0.2V	0.1		15.3	0.1		16	ns
			V_{CCB}=3.3V±0.3V	0.1		15.3	0.1		16	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V±0.1V	0.1		12.5	0.1		13.1	ns
			V_{CCB}=1.5V±0.1V	0.1		12.5	0.1		13.1	ns
			V_{CCB}=1.8V±0.15V	0.1		12.5	0.1		13.1	ns
			V_{CCB}=2.5V±0.2V	0.1		12.5	0.1		13.1	ns
			V_{CCB}=3.3V±0.3V	0.1		12.5	0.1		13.1	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V±0.1V	0.1		9.2	0.1		9.7	ns
			V_{CCB}=1.5V±0.1V	0.1		9.2	0.1		9.7	ns
			V_{CCB}=1.8V±0.15V	0.1		9.2	0.1		9.7	ns
			V_{CCB}=2.5V±0.2V	0.1		9.2	0.1		9.7	ns
			V_{CCB}=3.3V±0.3V	0.1		9.2	0.1		9.7	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V±0.1V	0.1		8.7	0.1		9.2	ns
			V_{CCB}=1.5V±0.1V	0.1		8.7	0.1		9.2	ns
			V_{CCB}=1.8V±0.15V	0.1		8.7	0.1		9.2	ns
			V_{CCB}=2.5V±0.2V	0.1		8.7	0.1		9.2	ns
			V_{CCB}=3.3V±0.3V	0.1		8.7	0.1		9.2	ns
Propagation Delay From Input (DIR) to Output (B)	t_{PHZ} t_{PLZ}	V_{CCA}=1.2V±0.1V	V_{CCB}=1.2V±0.1V	0.1		19.4	0.1		20.2	ns
			V_{CCB}=1.5V±0.1V	0.1		15.7	0.1		16.4	ns
			V_{CCB}=1.8V±0.15V	0.1		13.9	0.1		14.6	ns
			V_{CCB}=2.5V±0.2V	0.1		11.2	0.1		11.9	ns
			V_{CCB}=3.3V±0.3V	0.1		10.2	0.1		11	ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V±0.1V	0.1		18.6	0.1		19.3	ns
			V_{CCB}=1.5V±0.1V	0.1		14.9	0.1		15.5	ns
			V_{CCB}=1.8V±0.15V	0.1		13	0.1		13.6	ns
			V_{CCB}=2.5V±0.2V	0.1		9.8	0.1		10.3	ns
			V_{CCB}=3.3V±0.3V	0.1		8.5	0.1		9.1	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V±0.1V	0.1		18.7	0.1		19.5	ns
			V_{CCB}=1.5V±0.1V	0.1		14.7	0.1		15.3	ns
			V_{CCB}=1.8V±0.15V	0.1		12.8	0.1		13.4	ns
			V_{CCB}=2.5V±0.2V	0.1		9.5	0.1		10	ns
			V_{CCB}=3.3V±0.3V	0.1		8.2	0.1		8.8	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V±0.1V	0.1		18.3	0.1		19	ns
			V_{CCB}=1.5V±0.1V	0.1		14.2	0.1		14.8	ns
			V_{CCB}=1.8V±0.15V	0.1		12.1	0.1		12.7	ns
			V_{CCB}=2.5V±0.2V	0.1		9.2	0.1		9.7	ns
			V_{CCB}=3.3V±0.3V	0.1		7.8	0.1		8.3	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V±0.1V	0.1		18.2	0.1		18.9	ns
			V_{CCB}=1.5V±0.1V	0.1		14.5	0.1		15.1	ns
			V_{CCB}=1.8V±0.15V	0.1		12.5	0.1		13.1	ns
			V_{CCB}=2.5V±0.2V	0.1		9.1	0.1		9.6	ns
			V_{CCB}=3.3V±0.3V	0.1		7.7	0.1		8.2	ns

■ SWITCHING CHARACTERISTICS (Cont.)

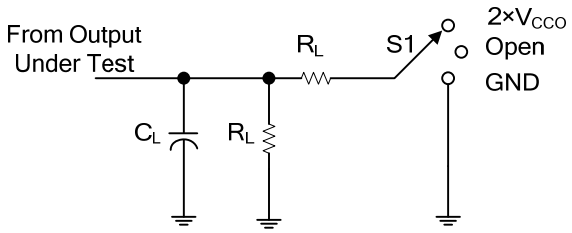
PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+85°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input (DIR) to Output (A)	t_{PZH} t_{PZL}	V_{CCA}=1.2V±0.1V	V_{CCB}=1.2V±0.1V			24.4			26.1	ns
			V_{CCB}=1.5V±0.1V			20.7			22.2	ns
			V_{CCB}=1.8V±0.15V			19.6			21.1	ns
			V_{CCB}=2.5V±0.2V			17.4			18.9	ns
			V_{CCB}=3.3V±0.3V			16.3			17.9	ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V±0.1V			20.4			21.8	ns
			V_{CCB}=1.5V±0.1V			16.3			17.5	ns
			V_{CCB}=1.8V±0.15V			15.1			16.3	ns
			V_{CCB}=2.5V±0.2V			12.5			13.5	ns
			V_{CCB}=3.3V±0.3V			12			13.1	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V±0.1V			18.8			20.3	ns
			V_{CCB}=1.5V±0.1V			14.3			15.4	ns
			V_{CCB}=1.8V±0.15V			13.2			14.3	ns
			V_{CCB}=2.5V±0.2V			10.4			11.3	ns
			V_{CCB}=3.3V±0.3V			9.9			10.9	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V±0.1V			17			18.3	ns
			V_{CCB}=1.5V±0.1V			12			13	ns
			V_{CCB}=1.8V±0.15V			10.5			11.5	ns
			V_{CCB}=2.5V±0.2V			8.2			9	ns
			V_{CCB}=3.3V±0.3V			8.6			9.4	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V±0.1V			16.3			17.7	ns
			V_{CCB}=1.5V±0.1V			11.1			12.1	ns
			V_{CCB}=1.8V±0.15V			9.6			10.6	ns
			V_{CCB}=2.5V±0.2V			7.7			8.5	ns
			V_{CCB}=3.3V±0.3V			7.1			7.9	ns
Propagation Delay From Input (DIR) to Output (B)	t_{PZH} t_{PZL}	V_{CCA}=1.2V±0.1V	V_{CCB}=1.2V±0.1V			24.8			26.6	ns
			V_{CCB}=1.5V±0.1V			21.6			23.2	ns
			V_{CCB}=1.8V±0.15V			19.9			21.5	ns
			V_{CCB}=2.5V±0.2V			18.5			20	ns
			V_{CCB}=3.3V±0.3V			16.9			18.5	ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V±0.1V			20.3			21.8	ns
			V_{CCB}=1.5V±0.1V			16.7			18	ns
			V_{CCB}=1.8V±0.15V			14.9			16.1	ns
			V_{CCB}=2.5V±0.2V			13			14.1	ns
			V_{CCB}=3.3V±0.3V			11.8			12.9	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V±0.1V			18.2			19.6	ns
			V_{CCB}=1.5V±0.1V			14.6			15.8	ns
			V_{CCB}=1.8V±0.15V			12.8			13.9	ns
			V_{CCB}=2.5V±0.2V			10.9			11.9	ns
			V_{CCB}=3.3V±0.3V			9.6			10.6	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V±0.1V			15.4			16.7	ns
			V_{CCB}=1.5V±0.1V			12.9			12.9	ns
			V_{CCB}=1.8V±0.15V			10.1			11	ns
			V_{CCB}=2.5V±0.2V			8.2			9	ns
			V_{CCB}=3.3V±0.3V			7.8			8.6	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V±0.1V			14.8			16.1	ns
			V_{CCB}=1.5V±0.1V			11.2			12.2	ns
			V_{CCB}=1.8V±0.15V			9.4			10.3	ns
			V_{CCB}=2.5V±0.2V			8.5			9.3	ns
			V_{CCB}=3.3V±0.3V			7.1			7.9	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Capacitance	Control Inputs	C_{IN}	V_{IN}=3.3V or GND, V_{CCA}=3.3V, V_{CCB}=3.3V			2.5		pF
Input/Output Capacitance	A or B Port	C_{IO}	V_{IN}=3.3V or GND, V_{CCA}=3.3V, V_{CCB}=3.3V			6		pF
Power Dissipation Capacitance	A Port Input B Port Output	C_{PDA}	C_L=0, f=10MHz t_r=t_f=1nS	V_{CCB}=1.2V		3		pF
				V_{CCB}=1.5V		3		pF
				V_{CCB}=1.8V		3		pF
				V_{CCB}=2.5V		3		pF
				V_{CCB}=3.3V		4		pF
	B Port Input A Port Output			V_{CCB}=1.2V		13		pF
				V_{CCB}=1.5V		13		pF
				V_{CCB}=1.8V		14		pF
				V_{CCB}=2.5V		15		pF
				V_{CCB}=3.3V		15		pF
	A Port Input B Port Output	C_{PDB}		V_{CCB}=1.2V		13		pF
				V_{CCB}=1.5V		13		pF
				V_{CCB}=1.8V		14		pF
				V_{CCB}=2.5V		14		pF
				V_{CCB}=3.3V		15		pF
	B Port Input A Port Output			V_{CCB}=1.2V		3		pF
				V_{CCB}=1.5V		3		pF
				V_{CCB}=1.8V		3		pF
				V_{CCB}=2.5V		3		pF
				V_{CCB}=3.3V		3		pF

Note: Power dissipation capacitance per transceiver.

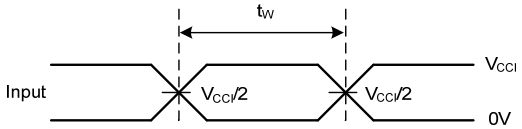
■ TEST CIRCUIT AND WAVEFORMS



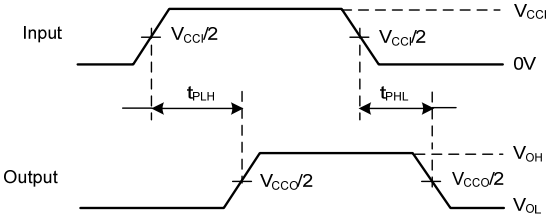
Load Circuit

TEST	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	$2\times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

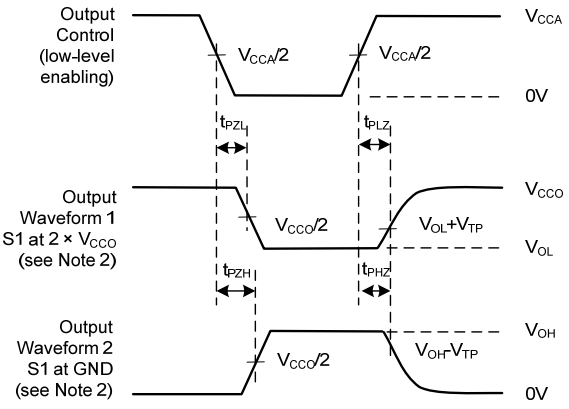
V_{CCO}	C_L	R_L	V_{TP}
1.2V±0.1V	15pF	2kΩ	0.1V
1.5V±0.1V	15pF	2kΩ	0.1V
1.8V±0.15V	15pF	2kΩ	0.15V
2.5V±0.2V	15pF	2kΩ	0.15V
3.3V±0.3V	15pF	2kΩ	0.3V



Pulse Duration



Propagation Delay Times



Enable and Disable Times

Notes: 1. C_L includes probe and jig capacitance.

2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50W, dv/dt ≥1 V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{PD}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

■ DETAILED DESCRIPTION

Overview

The **U74AVC1T45B** is single-bit, dual-supply, noninverting voltage level translation. Pin A and direction control pin are support by V_{CCA} and pin B is support by V_{CCB}. The A port is able to accept I/O voltages ranging from 0.8V to 3.6V, while the B port can accept I/O voltages from 0.8V to 3.6V. The high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A.

■ FEATURES DESCRIPTION

Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2V to 3.6V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the voltage nodes (1.2V, 1.8V, 2.5V and 3.3V).

I_{OFF} Supports Partial-Power-Down Mode Operation

I_{OFF} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

Enable Times

Calculate the enable times for the **U74AVC1T45B** using the following formulas:

* t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
* t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
* t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
* t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the **U74AVC1T45B** initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

■ POWER SUPPLY RECOMMENDATIONS

The **U74AVC1T45B** device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 0.8V to 3.6V and V_{CCB} accepts any supply voltage from 0.8V to 3.6V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage, bidirectional translation between any of the 1.2V, 1.5 V, 1.8V, and 3.3V voltage nodes.

Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

Table 1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}							UNIT
	0V	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	μA
0V	0	<0.5	<0.5	<0.5	<0.5	<0.5	<0.5	μA
0.8V	<0.5	<0.5	<0.5	<0.5	<0.5	<1	<2.5	μA
1.2V	<0.5	<0.5	<1	<1	<1	<1	1	μA
1.5V	<0.5	<0.5	<1	<1	<1	<1	1	μA
1.8V	<0.5	<0.5	<1	<1	<1	<1	<1	μA
2.5V	<0.5	<1	1	<1	<1	<1	<1	μA
3.3V	<0.5	<2.5	1	<1	<1	<1	<1	μA

■ TYPICAL APPLICATION CIRCUIT

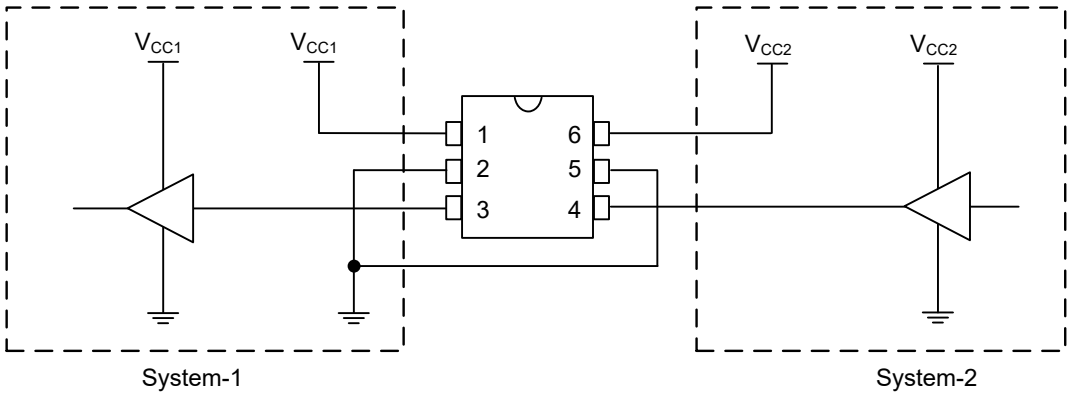


Figure 1. Unidirectional Logic Level-Shifting Application

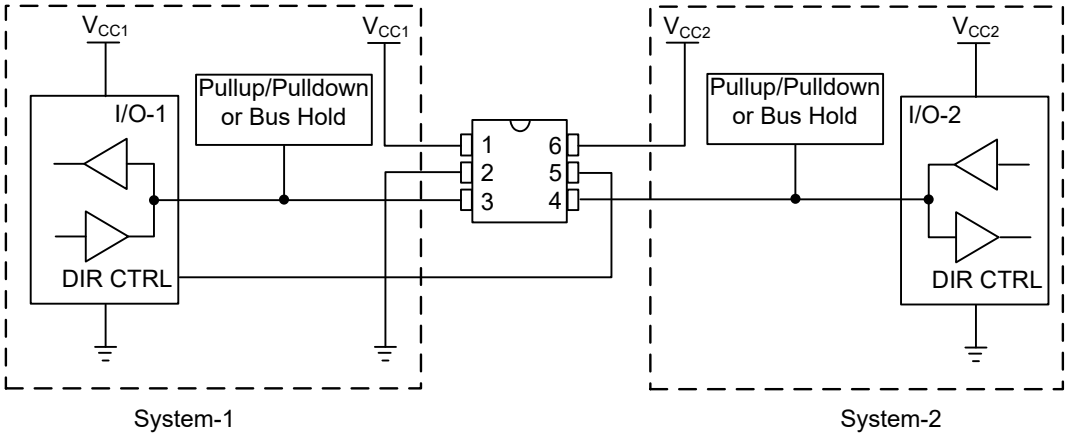


Figure 2. Bidirectional Logic Level-Shifting Application

Table 2.Data Transmission: SYSTEM-1 and SYSTEM-2

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	OUT	IN	SYSTEM-1 data to SYSTEM-2
2	H	HI-Z	HI-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus- line state depends on pullup or pulldown. (Note)
3	L	HI-Z	HI-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. (Note)
4	L	IN	OUT	SYSTEM-2 data to SYSTEM-1

Note: SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.