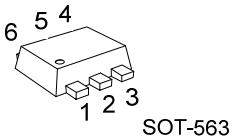
17V, 3A ,1.2MHZ SYNCHRONOUS STEP-DOWN CONVERTER



SOT-563

■ DESCRIPTION

The UTC **UD17301** is a fully integrated, highfrequency, synchronous, rectified, step-down, switchmode converter with internal power MOSFETs. The **UD17301** offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input range.

The **UD17301** uses synchronous-mode operation for higher efficiency over the output current-load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include shortcircuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

■ FEATURES

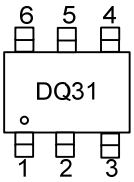
* Wide 4.2V to 17V Operating Input Range
* 63mΩ / 36mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
* 200μA Low I_Q
* High-Efficiency Synchronous Mode Operation
* Forced PWM Operation Mode
* Fast Load Transient Response
* 1.2MHz Switching Frequency
* Internal Soft Start (SS)
* Over-Current Protection (OCP) and Hiccup
* Thermal Shutdown
* Output Adjustable from 0.8V

■ ORDERING INFORMATION

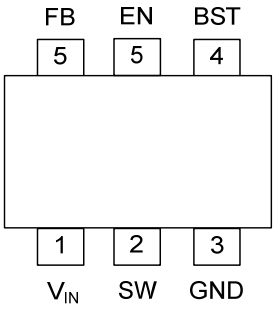
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD17301L-AN6-R	UD17301G-AN6-R	SOT-563	Tape Reel

UD17301G-AN6-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AN6: SOT-563 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



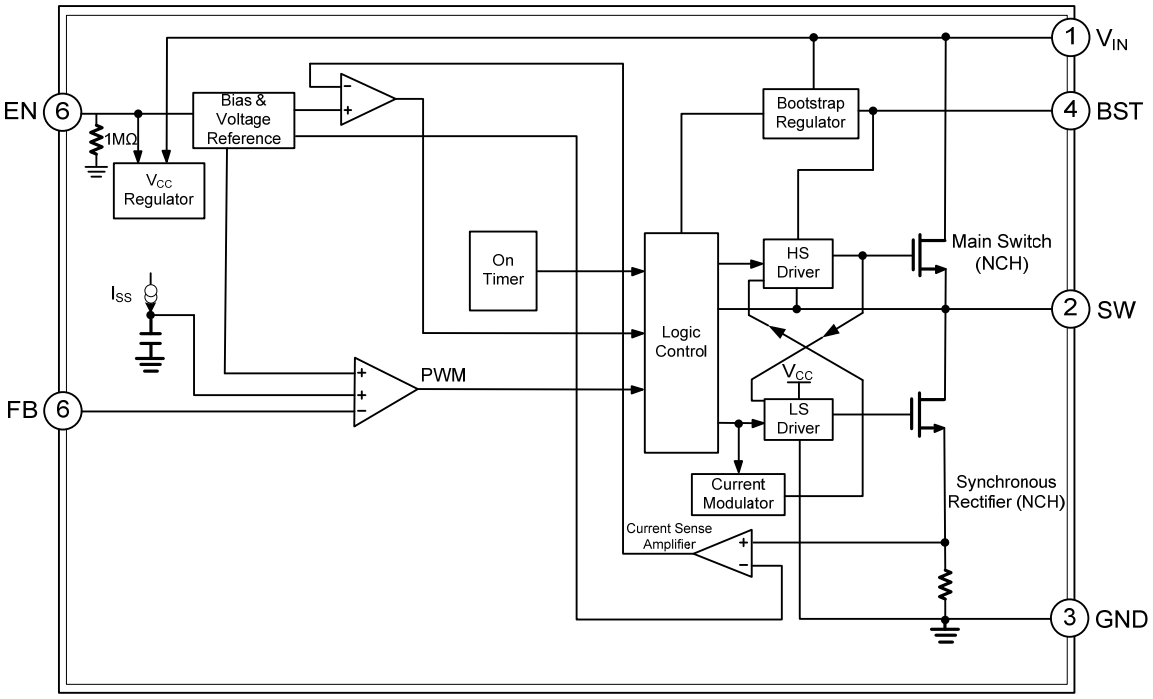
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{IN}	**Supply voltage**. The **UD17301** operates from a 4.2V to 17V input rail. A capacitor is required to decouple the input rail. Connect V_{IN} using a wide PCB trace.
2	SW	**Output switching node**. Connect SW using a wide PCB trace.
3	GND	**System ground**. GND is the reference ground of the regulated output voltage and requires extra care during the PCB layout. Connect GND with copper traces and vias.
4	BST	**Bootstrap**. Connect a 1μF BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
5	EN	**On/off control.** Drive EN high to enable the **UD17301**. For automatic start-up, connect EN to V_{IN} through a 100kΩ pull-up resistor.
6	FB	**Feedback**. Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	-0.3 ~ 18	V
SW to GND	V_{SW}	-0.6 (-6.5 for < 10ns) to V_{IN}+0.3 (19 for < 10ns)	V
BST to SW	V_{BST}	V_{SW} + 5	V
EN to GND	V_{EN}	-0.3 ~ 5	V
All other pins		-0.3 ~ 5	V
Continuous Power Dissipation (T_A=25°C)	P_{CNT}	2.2	W
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	4.2 ~ 17	V
V_{OUT} to GND	V_{OUT}	0.8V to Dmax x or 10V max	V
Operation junction Temperature Range	T_J	-40 ~ +125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	55	°C/W
Junction to Case	θ_{JC}	21	°C/W

Note: Measured on 2-layer PCB, 64mm×48mm.

■ ELECTRICAL CHARACTERISTICS (V_{IN}=12V, T_A=-40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UVLO AND QUIESCENT CURRENT						
V_{IN} UVLO Up Threshold	V_{IN_UVU}		3.7	4.0	4.18	V
V_{IN} UVLO Hysteresis	$V_{IN\_UV\_Hys}$			330		mV
Quiescent Supply Current	I_Q	V_{EN}= 2V, V_{FB}=0.85V	0.17	0.2	0.25	mA
Shutdown Current	I_{SD}	V_{EN}= 0V			10	μA
Switch Leakage Current	SW_{LKG}	V_{EN}= 0V, V_{SW}=12V			10	μA
FEEDBACK VOLTAGE						
Feedback Voltage	V_{FB}	T_J=25°C	0.793	0.805	0.817	V
		T_J=-40°C to +125°C	0.785	0.805	0.825	V
Feedback Current	I_{FB}			10	100	nA
FB UV Threshold (H to L)	V_{UV_TH}	Hiccup entry		44%		V_{REF}
Hiccup Duty Cycle (Note 2)	D_{Hiccup}			25		%
OC Hiccup Deglitch Time	T_{OC_DEG}					ms
POWER STAGE						
High-Side Switch on Resistance	R_{ON_HSmos}	V_{BST}-SW = 3.3V		63		mΩ
Low-Side Switch on Resistance	R_{ON_LSmos}			36		mΩ
CURRENT LIMIT						
Valley Current Limit	I_{LIM}	V_{OUT}=0V		4		A
SOFT START						
Soft-Start time	T_{SS}		1.6	2.5	3.0	ms
SWITCHING FREQUENCY/SYNC FUNCTION						
Oscillator frequency	F_{SW}	V_{FB}=0.75V	1000	1200	1500	kHz
Minimum On Time (Note 2)	T_{ON_MIN}			45		ns
Minimum OFF Time (Note 2)	T_{OFF_MIN}			180		ns
ENABLE						
Enable Rising Threshold	V_{EN_R}		1.14	1.2	1.26	V
Enable Threshold Hysteresis	V_{EN_Hys}			0.1		mV
Enable Input Current	I_{EN}	V_{EN}=2V		2		μA
THERMAL PROTECTION						
Thermal Shutdown (Note 2)	T_{OTP_R}			150		°C
Thermal Hysteresis (Note 2)	T_{OTP_Hys}			20		°C

Notes: 1. Guaranteed by over-temperature correlation, not tested in production.
2. Guaranteed by design and engineering sample characterization.

■ FUNCTION DESCRIPTION

The **UD17301** is a fully integrated, synchronous, rectified, step-down, switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HSFET) is turned on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}).

The HS-FET is turned on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off until the next period. By repeating operation this way, the converter regulates the output voltage.

The low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time is generated internally between the HS-FET off and LSFET on period or the LS-FET off and HS-FET on period.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to float to shut down the IC.

EN is clamped internally using a 2.8V series Zener diode (see Figure 1). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 100μA, preventing damage to the Zener diode. For example, if connecting a 100kΩ pull-up resistor to 12V V_{IN}, then I_{Zener} = (12V - 2.8V) / (100kΩ + 35kΩ) = 68μA.

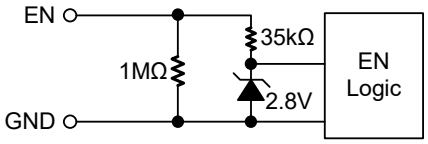


Figure 1. Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The **UD17301** UVLO comparator monitors the output voltage of the internal regulator (V_{CC}). The UVLO rising threshold is about 4V, while its falling threshold is 3.67V consistently.

Internal Soft Start (SS)

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 2.5ms internally.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The **UD17301** has a valley current-limit control. During the LS-FET on state, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the low-side limit comparator turns over, the **UD17301** enters over-current protection (OCP) mode, and the HS-FET waits until the valley current limit is removed before turning on again. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 44% below the reference). Once UV is triggered, the **UD17301** enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still remains after the soft start ends, the device repeats this operation cycle until the over-current condition is removed. The output rises back to the regulation level. OCP is a non-latch protection.

■ FUNCTION DESCRIPTION (Cont.)

Pre-Bias Start-Up

The **UD17301** is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the **UD17301** starts working normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. VIN regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1, and C2 (see Figure 2). If V_{IN} - V_{SW} exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C3.

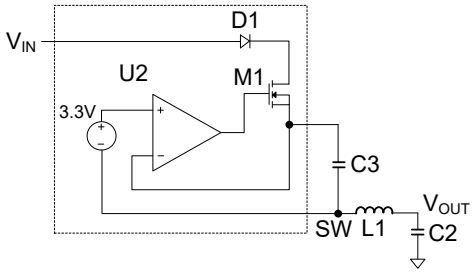


Figure 2. Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The internal supply rail is then pulled down.

■ APPLICATION INFORMATION

Start-Up and Shutdown Circuit

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise-sensitive. R2 is recommended be within 5 - 100kΩ. Typically, set the current through R2 to be between 5 - 30μA for a good balance between system stability and no-load loss. Then determine R1 with Equation (1):

$$R1=\frac{V_{OUT}-V_{REF}}{V_{REF}}\times R2 \quad (1)$$

The feedback circuit is shown in Figure 3.

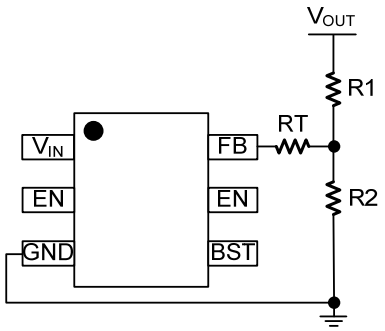


Figure. 3 Feedback Network

Table 1. Recommended parameters for common output voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
5	40.2	7.68	75	2.2
3.3	40.2	13	75	1.5
2.5	40.2	19.1	100	1.5
1.8	40.2	32.4	110	1.2
1.5	40.2	45.3	249	1
1.2	40.2	82	249	0.68
1	20.5	84.5	348	0.68

Note: Parameters Selection for Common Output Voltages, C_{OUT} = 22μF×2.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 - 60% of the maximum output current. The inductance value can be calculated with Equation (2):

$$L=\frac{V_{OUT}}{F_{SW}\times\Delta I_L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (3):

$$I_{LP}=I_{OUT}+\frac{V_{OUT}}{2\times F_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

■ APPLICATION INFORMATION(Cont.)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (4):

$$I_{CIN}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2V_{OUT}, shown in Equation (5):

$$I_{CIN}=\frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (6):

$$\Delta V_{IN}=\frac{I_{OUT}}{F_{SW}C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

The worst-case condition occurs at V_{IN} = 2V_{OUT}, shown in Equation (7):

$$\Delta V_{IN}=\frac{1}{4}\times\frac{I_{OUT}}{F_{SW}C_{IN}} \quad (7)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times F_{SW}\times C_{OUT}}\right) \quad (8)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times F_{SW}^{2}\times L\times C_{OUT}}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

The output voltage ripple caused by the ESR is very small.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR} \quad (10)$$

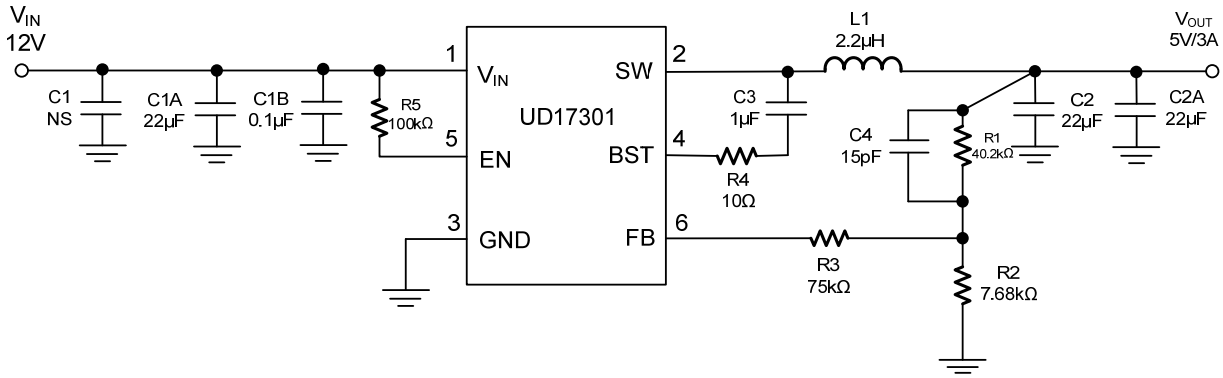
A larger output capacitor also can achieve a better load transient response, but be sure to consider the maximum output capacitor limitation in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value (C_{O_MAX}) can be limited approximately with Equation (11):

$$C_{O\_MAX}=\frac{I_{LIM\_AVG}-I_{OUT}}{V_{OUT}}\times T_{SS} \quad (11)$$

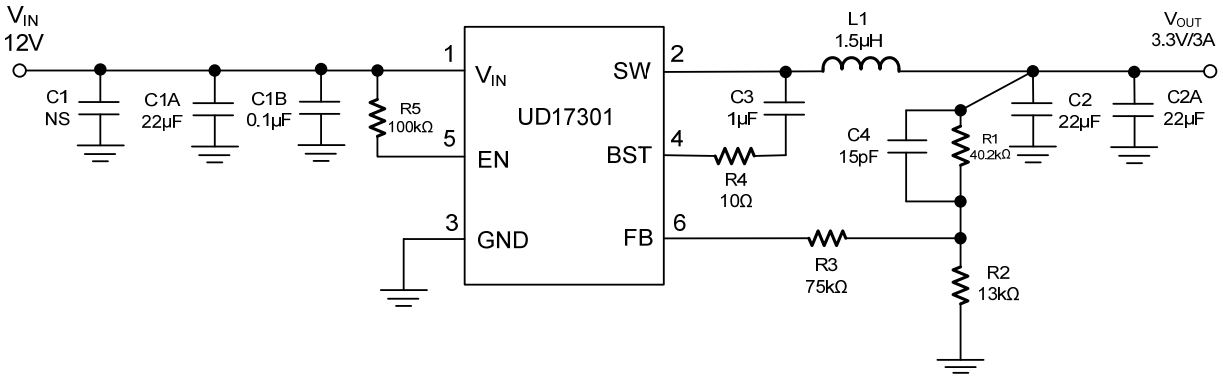
Where I_{LIM_AVG} is the average start-up current during the soft-start period, and TSS is the soft start time.

■ TYPICAL APPLICATION CIRCUIT

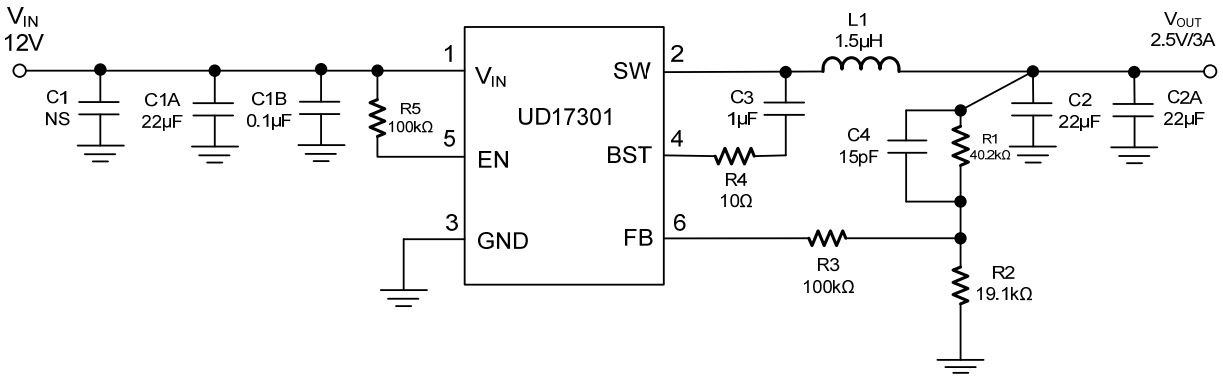
12V$_{IN}$, 5V/3A Output



12V$_{IN}$, 3.3V/3A Output

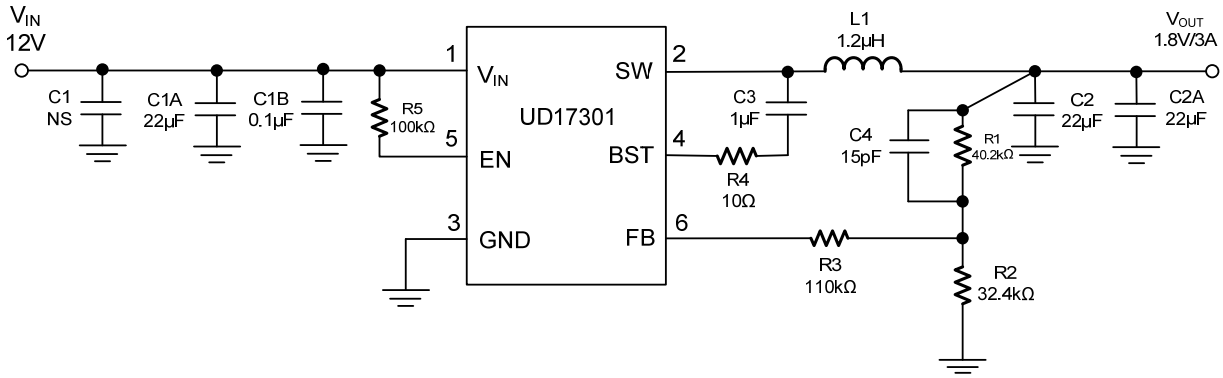


12V$_{IN}$, 2.5V/3A Output

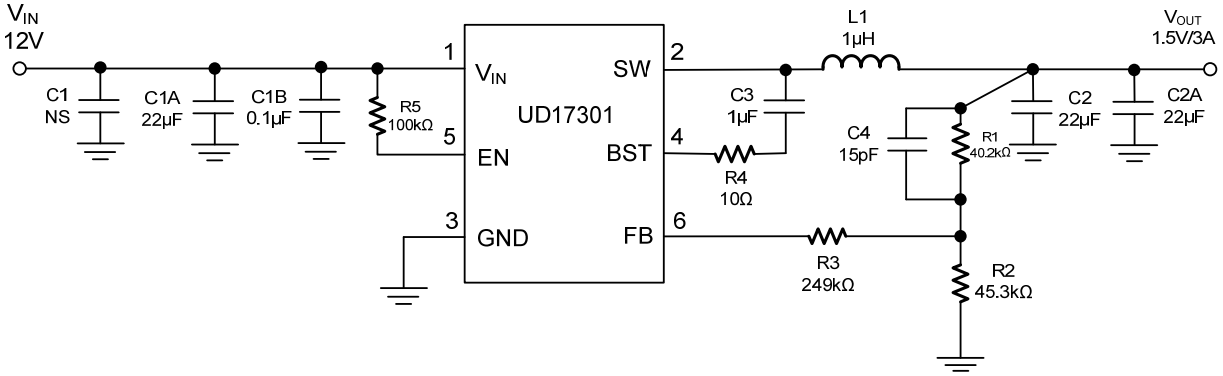


■ TYPICAL APPLICATION CIRCUIT(Cont.)

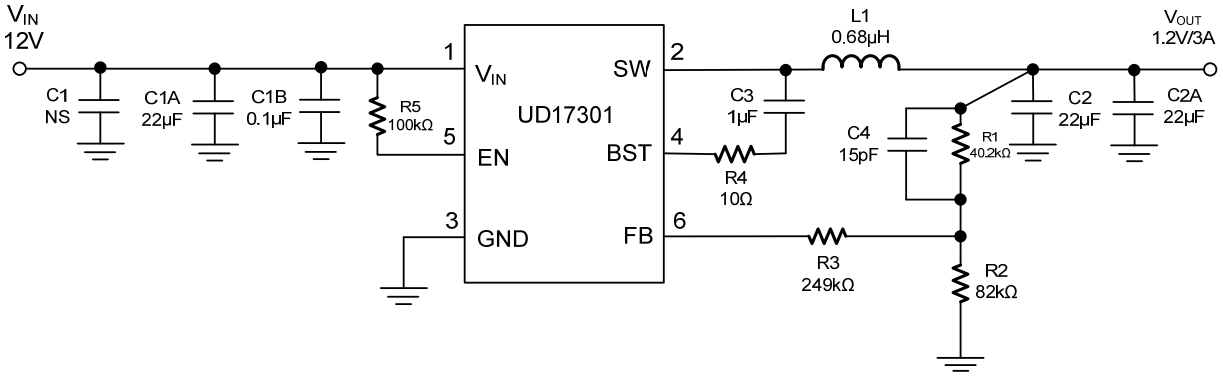
12V$_{IN}$, 1.8V/3A Output



12V$_{IN}$, 1.5V/3A Output



12V$_{IN}$, 1.2V/3A Output



■ TYPICAL APPLICATION CIRCUIT(Cont.)

12V_{IN}, 1V/3A Output