



USG10R080M

Preliminary

Power MOSFET

N-CHANNEL SGT ENHANCEMENT POWER MOSFET

DESCRIPTION

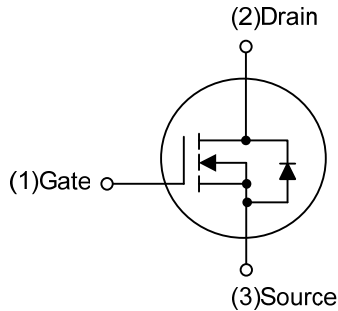
The UTC **USG10R080M** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with high switching speed and low gate charge, etc.

The UTC **USG10R080M** applies to primary side switch, synchronous rectifier, Motor Drives, etc.

FEATURES

- * $R_{DS(ON)} \leq 8.0 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
 $R_{DS(ON)} \leq 10 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=20\text{A}$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL

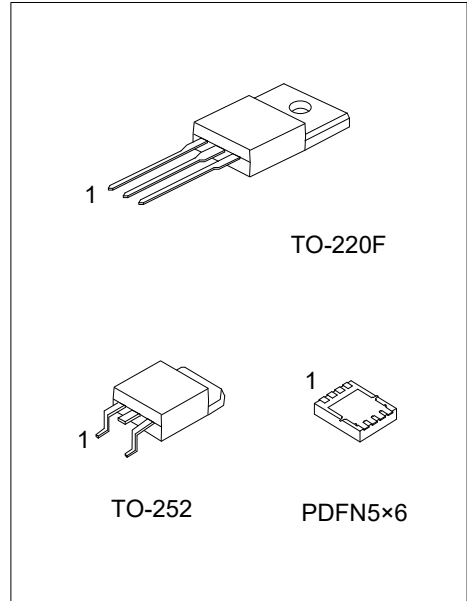


ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
USG10R080ML-TF3-T	USG10R080MG-TF3-T	TO-220F	G	D	S	-	-	-	-	-	Tube
USG10R080ML-TN3-R	USG10R080MG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
USG10R080ML-P5060-R	USG10R080MG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

USG10R080MG-TF3-T		(1)Packing Type	(1) T: Tube, R: Tape Reel
		(2)Package Type	(2) TF3: TO-220F3, TN3: TO-252, P5060: PDFN5×6
		(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING

TO-220F	TO-252
Diagram of TO-220F marking: A rectangular box contains 'UTC' and 'USG10R080M' above a row of six squares. The first square is labeled 'Lot Code' with an arrow pointing left. The last square is labeled 'Date Code' with an arrow pointing right. Below the squares is a '1'. To the right of the box, 'L: Lead Free' and 'G: Halogen Free' are listed with arrows pointing to the last square.	Diagram of TO-252 marking: A rectangular box contains 'UTC' and 'USG' above '10R080M' and a row of six squares. The first square is labeled 'Lot Code' with an arrow pointing left. The last square is labeled 'Date Code' with an arrow pointing right. Below the squares is a '1'. To the right of the box, 'L: Lead Free' and 'G: Halogen Free' are listed with arrows pointing to the last square.
PDFN5×6	-
Diagram of PDFN5x6 marking: A rectangular box contains 'UTC' and 'USG' above '10R080M' and a row of six squares. The first square is labeled 'Lot Code' with an arrow pointing left. The last square is labeled 'Date Code' with an arrow pointing right. A dot is located to the left of the second square.	-

■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	80	A
	Pulsed (Note 2)	I_{DM}	160	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.6	V/ns
Power Dissipation	TO-220F	P_D	36	W
	TO-252		54	W
	PDFN5×6		46	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 10\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, $T_J \leq T_{JMAX}$, $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F	θ_{JA}	62.5	$^\circ\text{C/W}$
	TO-252		110	$^\circ\text{C/W}$
	PDFN5×6		65 (Note)	$^\circ\text{C/W}$
Junction to Case	TO-220F	θ_{JC}	3.47	$^\circ\text{C/W}$
	TO-252		2.3 (Note)	$^\circ\text{C/W}$
	PDFN5×6		2.71 (Note)	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

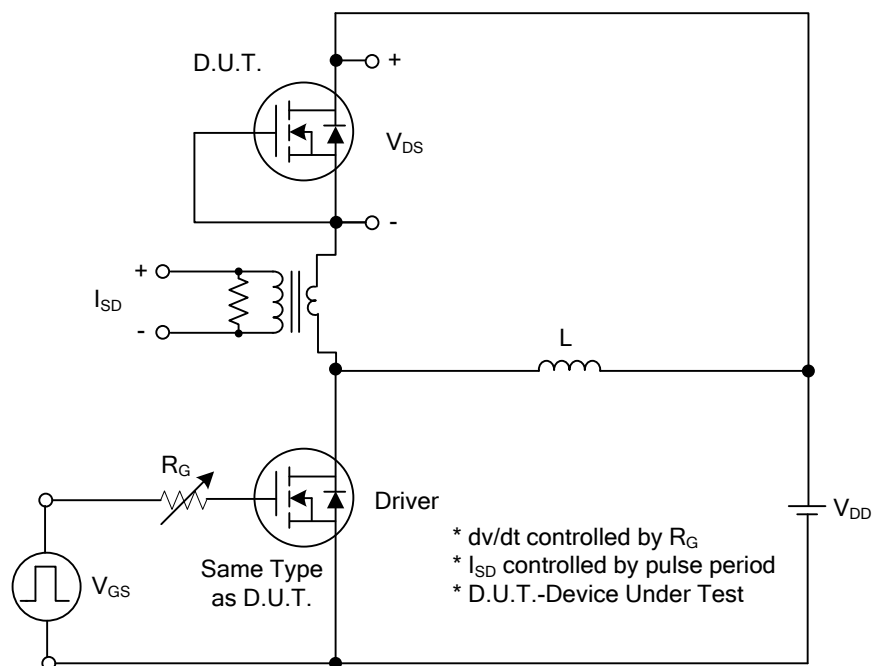
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A			8.0	mΩ
			V _{GS} =4.5V, I _D =20A			10	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		3022		pF
Output Capacitance		C _{OSS}			1266		pF
Reverse Transfer Capacitance		C _{RSS}			189		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =80V, V _{GS} =10V, I _D =100A		81		nC
Gate to Source Charge		Q _{GS}			11		nC
Gate to Drain Charge		Q _{GD}			30		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =50V, V _{GS} =10V, I _D =100A, R _G =3Ω		13		ns
Rise Time		t _R			21		ns
Turn-OFF Delay Time		t _{D(OFF)}			51		ns
Fall-Time		t _F			25		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				100	A
Drain-Source Diode Forward Voltage		V _{SD}	I _{SD} =75A			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =30A, dI/dt=100A/μs		52		ns
Body Diode Reverse Recovery Charge		Q _{rr}			81		nC

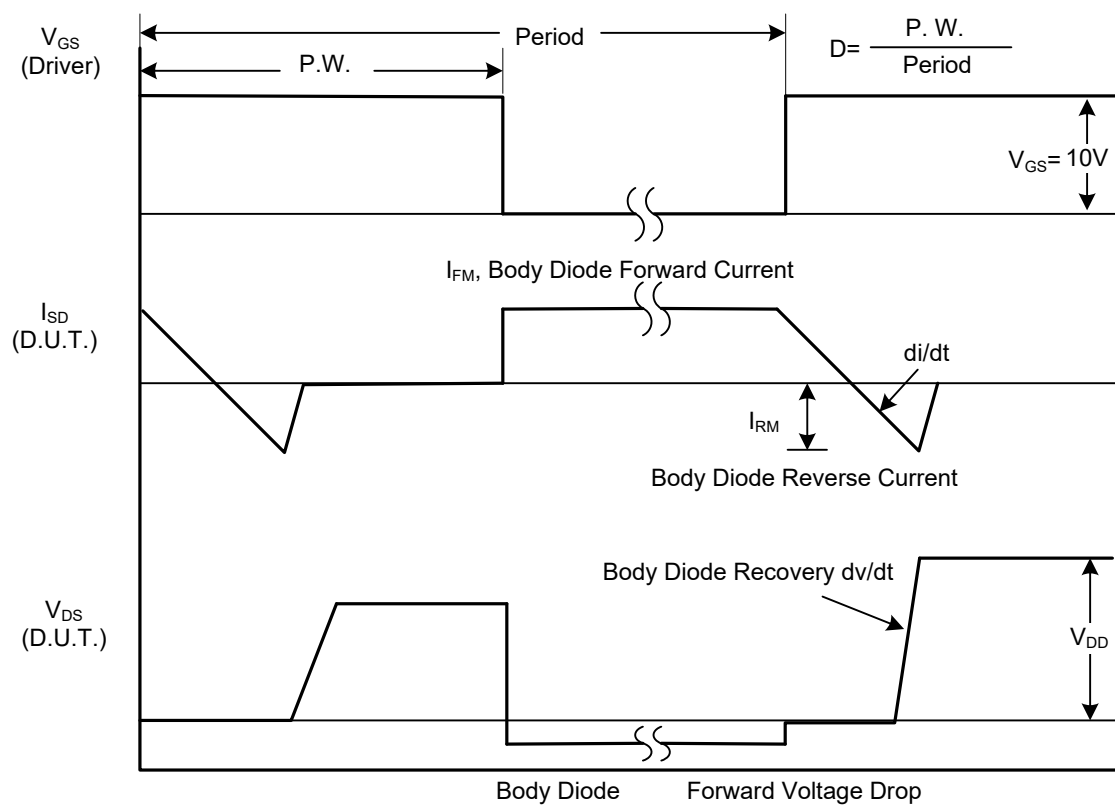
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

TEST CIRCUITS AND WAVEFORMS

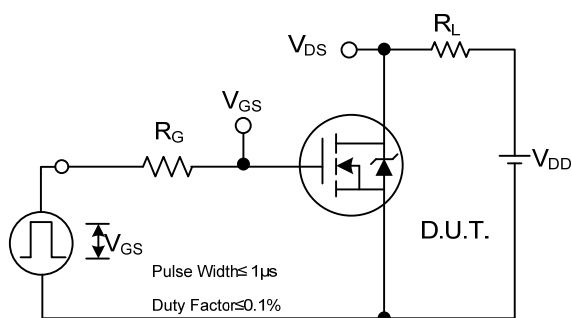


Peak Diode Recovery dv/dt Test Circuit

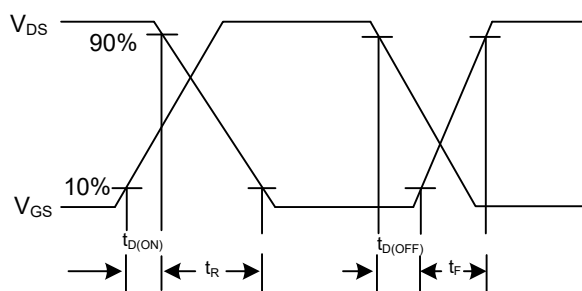


Peak Diode Recovery dv/dt Waveforms

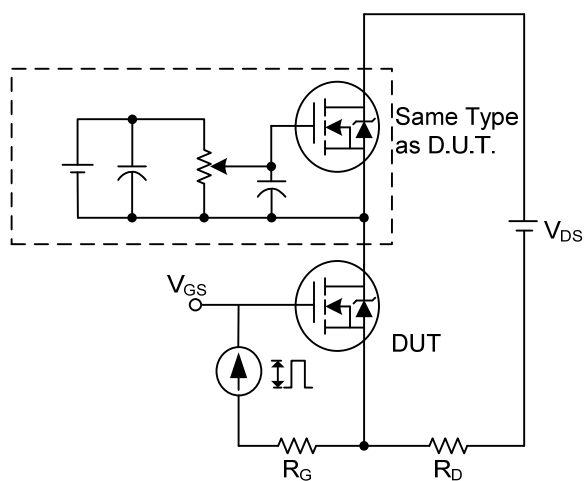
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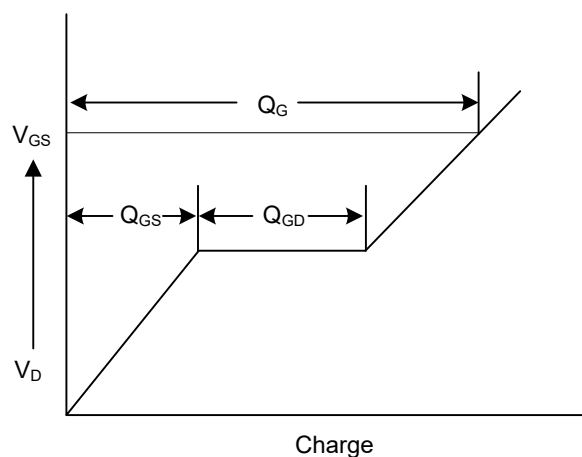
Switching Test Circuit



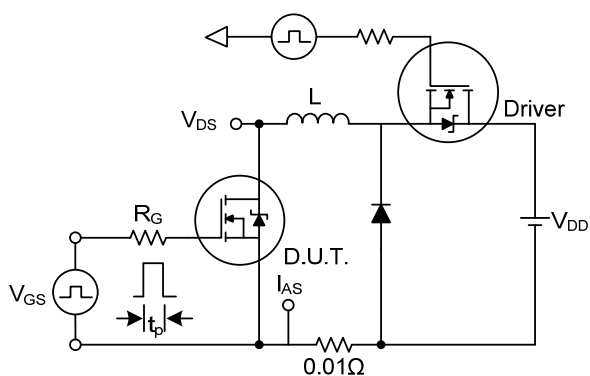
Switching Waveforms



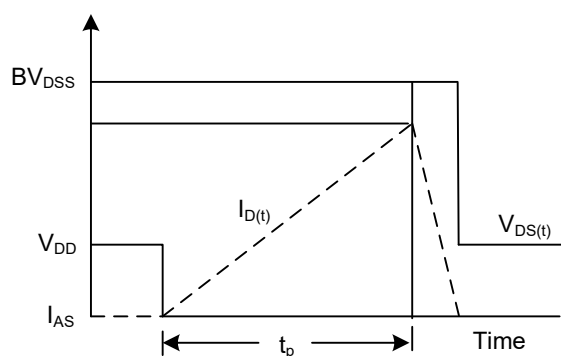
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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