



UT11N10M

Power MOSFET

11A, 100V N-CHANNEL POWER MOSFET

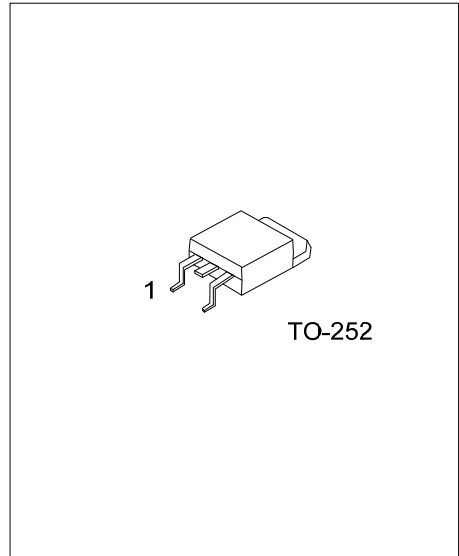
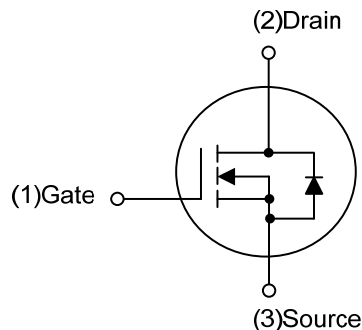
DESCRIPTION

The UTC **UT11N10M** is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

FEATURES

- * $R_{DS(ON)} \leq 115 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=5.5\text{A}$
- * $R_{DS(ON)} \leq 136 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=5.5\text{A}$
- * Improved dv/dt capability
- * High Switching Speed
- * Fast switching

SYMBOL



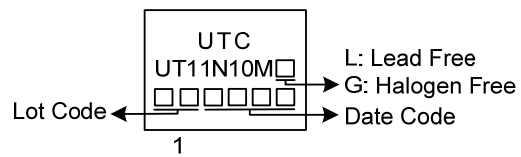
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT11N10ML-TN3-R	UT11N10MG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT11N10MG-TN3-R		(1)Packing Type	(1) R: Tape Reel
		(2)Package Type	(2) TN3: TO-252
		(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous ($V_{GS}=10\text{V}$)	I_D	11	A
	Pulsed (Note 2)	I_{DM}	22	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	0.3	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4	V/ns
Power Dissipation		P_D	43	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 2.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 11\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.5 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

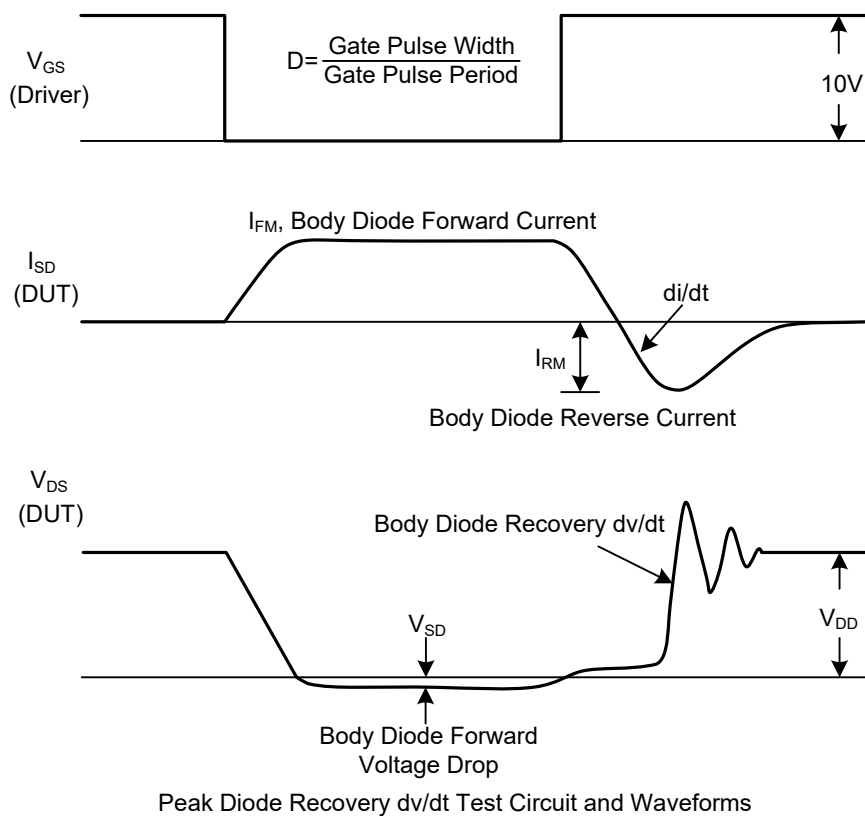
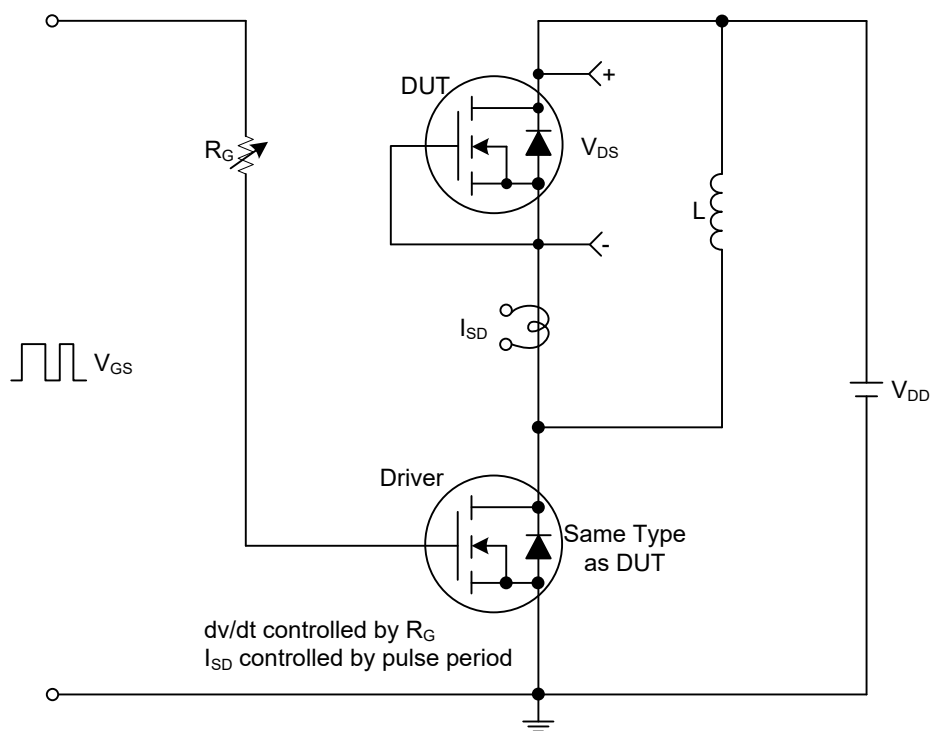
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V , I _D =5.5A			115	mΩ
			V _{GS} =4.5V, I _D =5.5A			136	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		579		pF
Output Capacitance		C _{OSS}			41		pF
Reverse Transfer Capacitance		C _{RSS}			32		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =80V, V _{GS} =10V, I _D =11A (Note 2)		22		nC
Gate to Source Charge		Q _{GS}			2		nC
Gate to Drain Charge		Q _{GD}			6		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =50V, V _{GS} =10V, I _D =11A, R _G =3Ω (Note 2)		4		ns
Rise Time		t _R			17		ns
Turn-OFF Delay Time		t _{D(OFF)}			15		ns
Fall-Time		t _F			18		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				11	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				22	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =11A,V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _F =11A,V _{GS} =0V, di/dt=100A/μs		120		ns
Body Diode Reverse Recovery Charge		Q _{rr}			133		nC

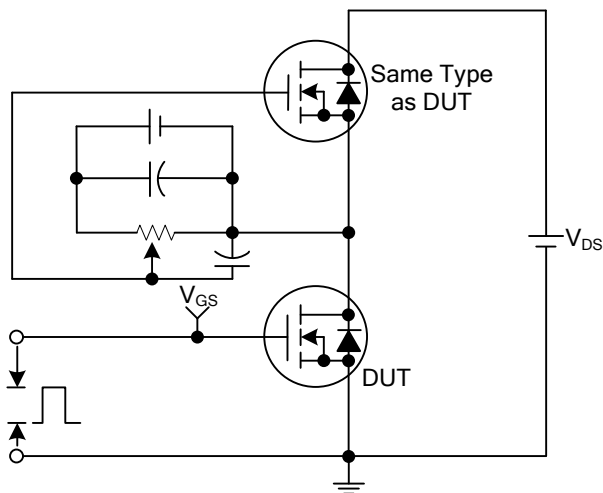
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

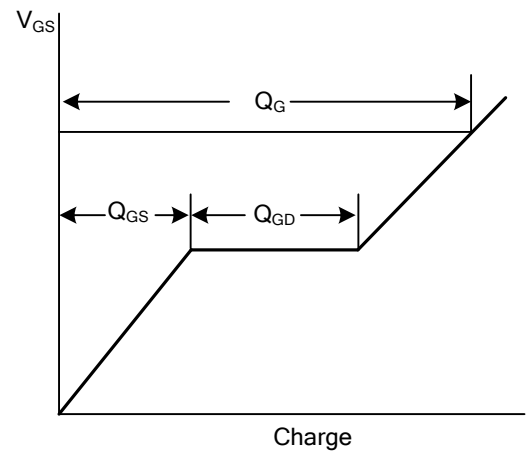
■ TEST CIRCUITS AND WAVEFORMS



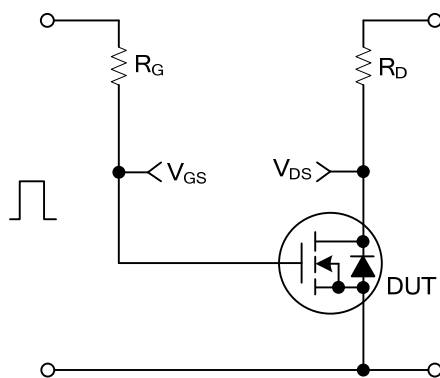
■ TEST CIRCUITS AND WAVEFORMS



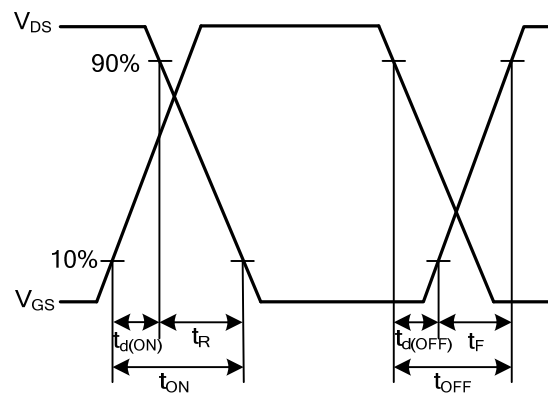
Gate Charge Test Circuit



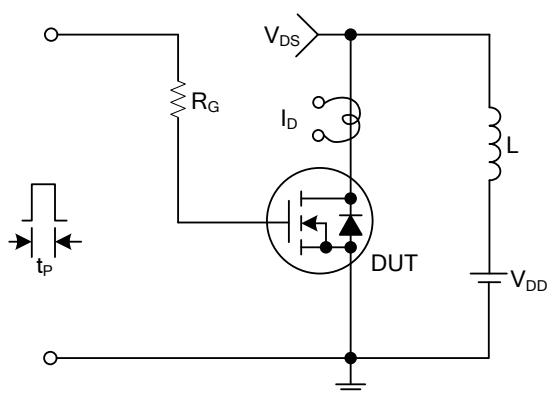
Gate Charge Waveforms



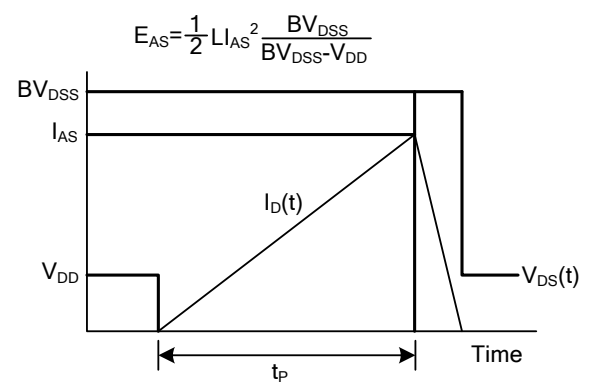
Resistive Switching Test Circuit



Resistive Switching Waveforms

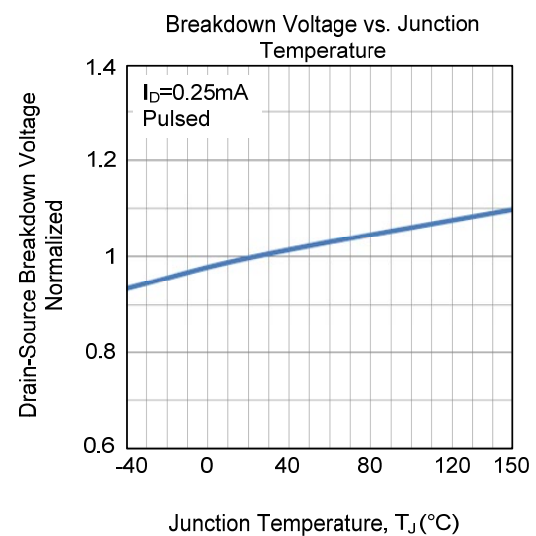
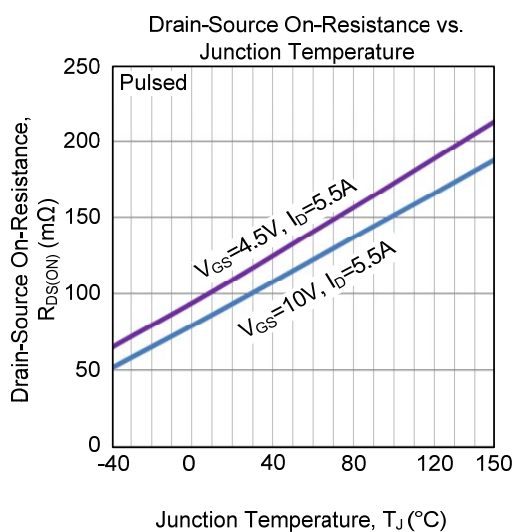
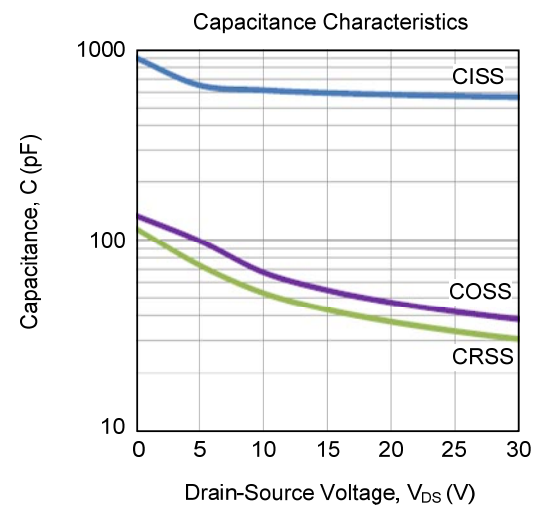
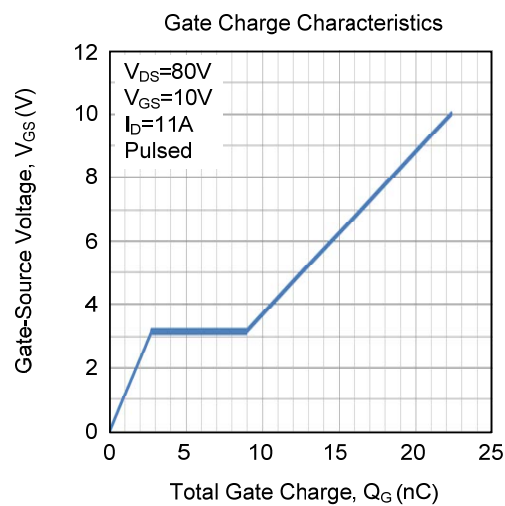
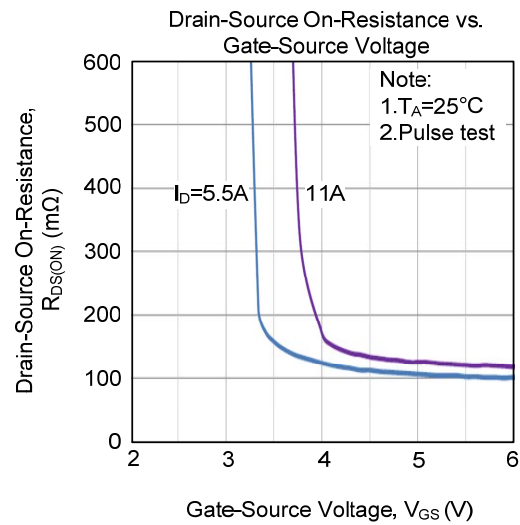
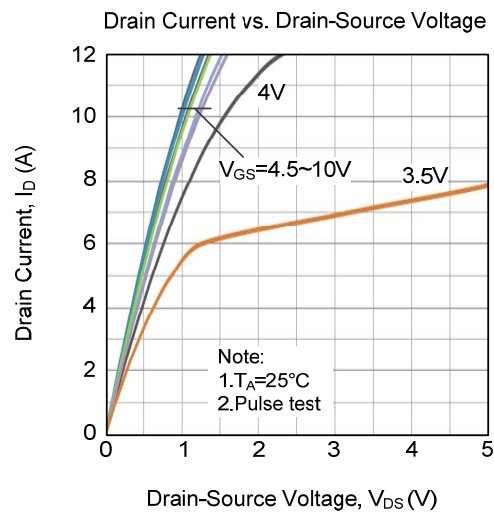


Unclamped Inductive Switching Test Circuit

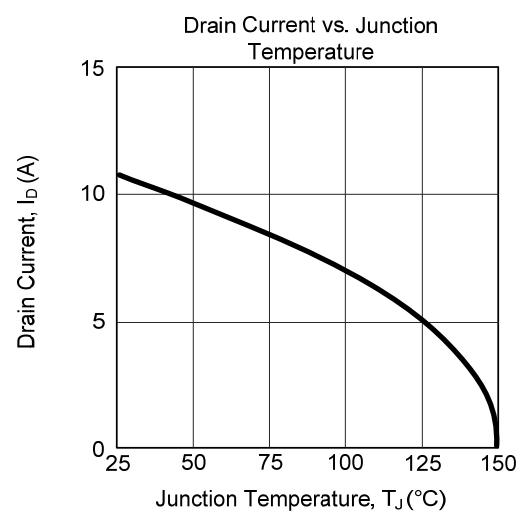
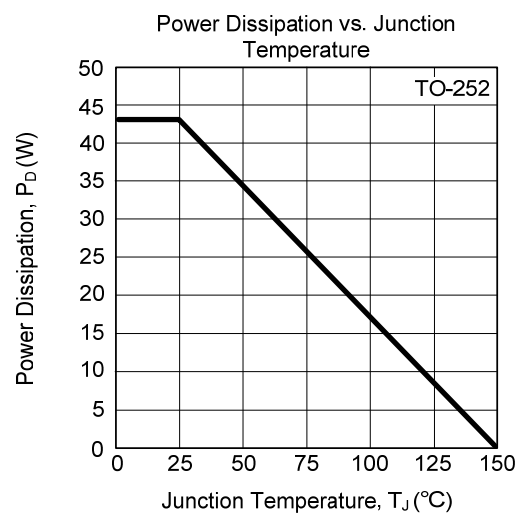
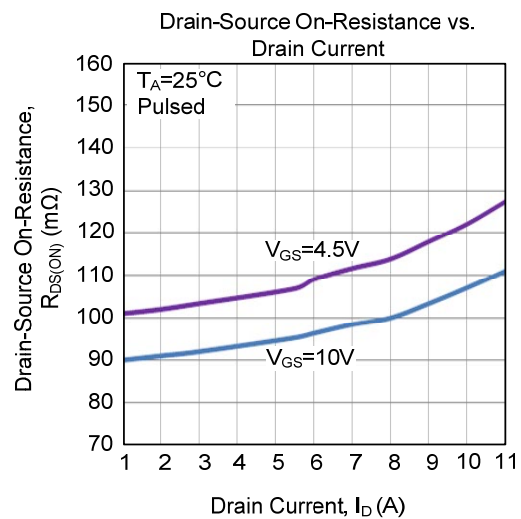
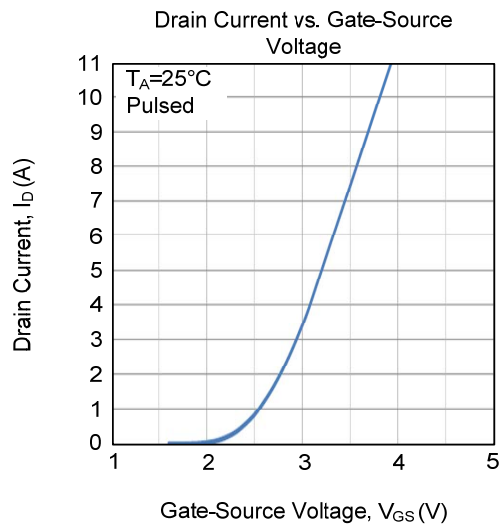
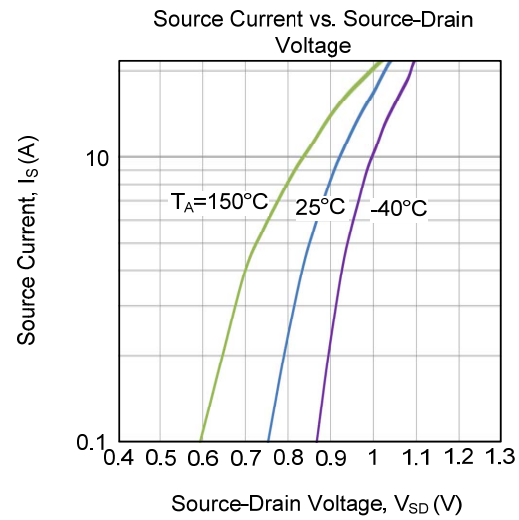
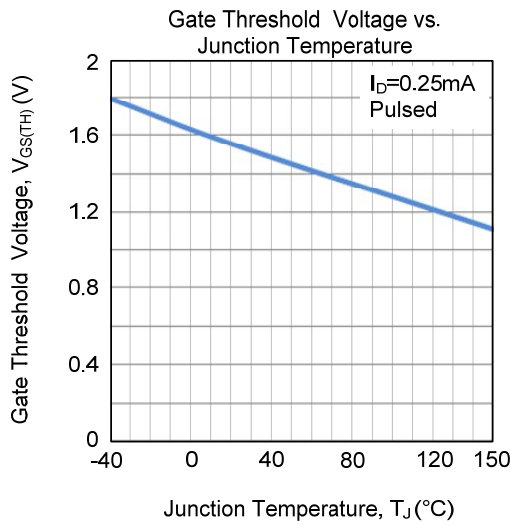


Unclamped Inductive Switching Waveforms

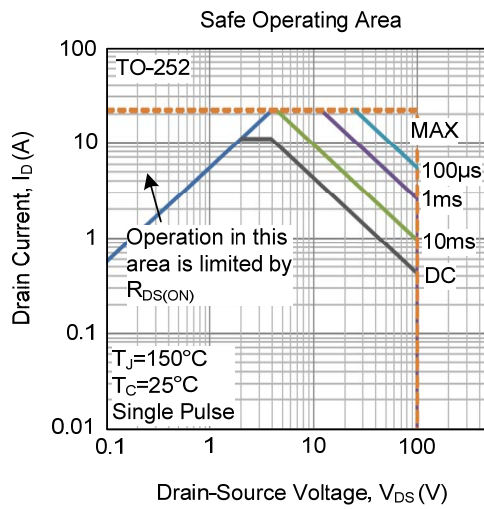
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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