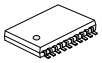
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



TSSOP-20U

■ DESCRIPTION

The UTC **U74HCT573E** are octal D-type transparent latches featuring separate D-type inputs for each latch and non-inverting 3-state outputs for bus-oriented applications.

■ FEATURES

* Operation Voltage Range: 4.5V~5.5V
* 3-state Non-Inverting Outputs for Bus-oriented Applications
* Common 3-state Output Enable Input
* Inputs are TTL voltage compatible

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT573EL-ULA-R	U74HCT573EG-ULA-R	TSSOP-20U	Tape Reel

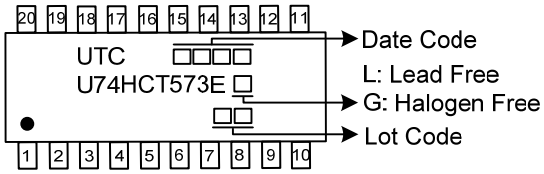
U74HCT573EG-ULA-R

(1)Packing Type — (1) R: Tape Reel

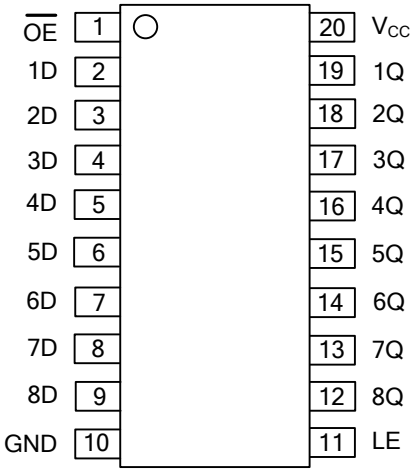
(2)Package Type — (2) ULA: TSSOP-20U

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



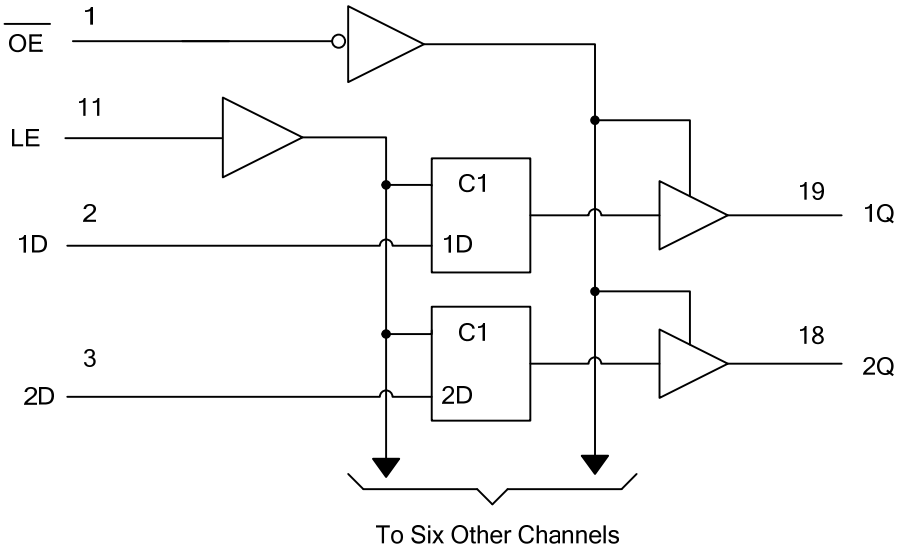
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS($\overline{OE}$)	INPUTS(LE)	INPUTS(D)	OUTPUT(Q)
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING(unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7.0	V
Input Clamp Current (Note 2)	I_{IK}	V_{IN}<0 or V_{IN}>V_{CC}	±20	mA
Output Clamp Current (Note 2)	I_{OK}	V_{OUT}<0 or V_{OUT}>V_{CC}	±20	mA
Output Current	I_{OUT}	V_{OUT}= 0 to V_{CC}	±35	mA
V_{CC} or GND Current	I_{CC}		±70	mA
Electrostatic Discharge	$V_{(ESD)}$	Human-Body Model (HBM) Per JESD22-A114/115	2000	V
Storage Temperature	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Time	t_R / t_F				500	ns
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS(T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=4.5V~5.5V	2.0			V
Low-Level Input Voltage	V_{IL}	V_{CC}=4.5V~5.5V			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98	4.1		V
Low-Level Output Voltage	V_{OL}	V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, I_{OL}=6mA		0.21	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=V_{CC} or GND			±100	nA
Output OFF -State Current	I_{OZ}	V_{CC}=5.5V, V_{OUT}=V_{CC} or GND			±0.5	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8	μA
Additional Quiescent Supply Current	△I_{CC}	V_{CC}=5.5V,One input at 0.5V or 2.4V, other inputs at 0 or V_{CC}			2.4	mA
Input Capacitance	C_{IN}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND			10	pF

■ TIMING REQUIREMENTS (T_A=25°C,unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse Duration, LE High	t_W	V_{CC}=4.5V	20			ns
Setup Time, Data Before LE↓	t_{SU}	V_{CC}=4.5V	13			ns
Hold Time, Data After LE↓	t_H	V_{CC}=4.5V	9			ns

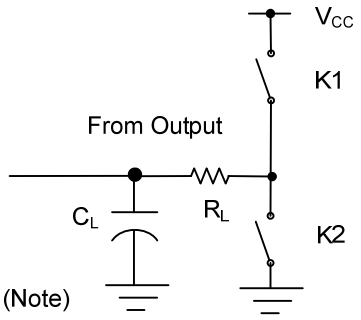
■ DYNAMIC CHARACTERISTICS (T_A=25°C, C_L=50pF,R_L=1kΩ,unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (D) To Output (Q)	t_{PD} (t_{PLH}/t_{PHL})	V_{CC}=4.5V		20	35	ns
Propagation Delay From Input (LE) To Output (Q)	t_{PD} (t_{PLH}/t_{PHL})	V_{CC}=4.5V		18	35	ns
3-State Output Enable Time From Input ($\overline{OE}$) To Output (Q)	t_{EN} (t_{PZL}/t_{PZH})	V_{CC}=4.5V		17	35	ns
3-State Output Disable Time From Input ($\overline{OE}$) To Output (Q)	t_{DIS} (t_{PLZ}/t_{PHZ})	V_{CC}=4.5V		18	35	ns
Output transition time, (Q)	t_T (t_{TLH}/t_{THL})	V_{CC}=4.5V			12	ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		50		pF

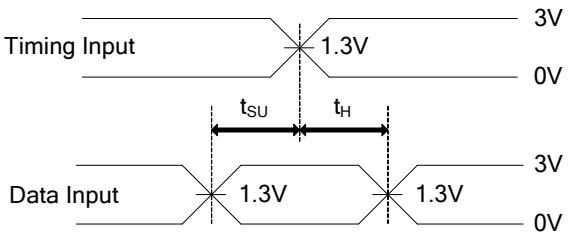
■ TEST CIRCUIT AND WAVEFORMS



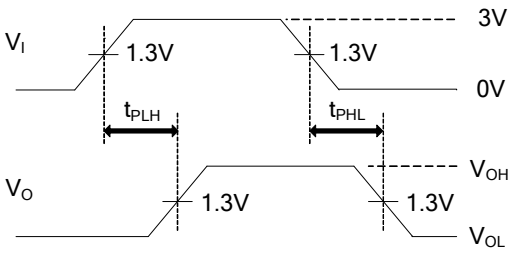
TEST	K1	K2
t_{PLH}/ t_{PHL}	Open	Open
t_{PHZ}/ t_{PZH}	Open	Close
t_{PLZ}/ t_{PZL}	Close	Open

Note: C_L includes probe and jig capacitance.

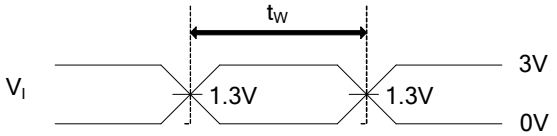
P_{RR} ≤1MHz, Z_O = 50Ω, t_R ≤6ns, t_F ≤6ns



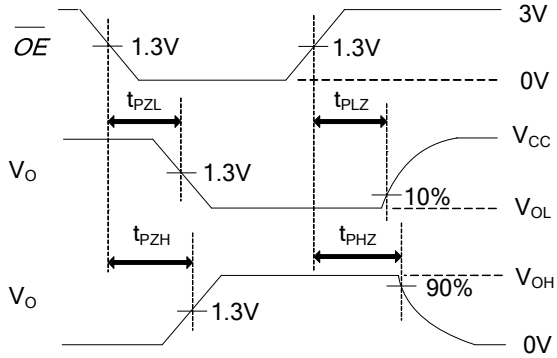
Setup Time and Hold Time



Propagation Delay Times



Pulse Width



Enable and Disable Times