

**UCD4040B**

Preliminary

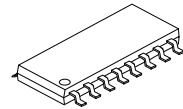
CMOS IC

CMOS RIPPLE-CARRY BINARY COUNTER/DIVIDERS**DESCRIPTION**

The **UCD4040B** are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

FEATURES

- * Medium-speed operation Fully static operation
- * Buffered inputs and outputs
- * 100% tested for quiescent current at 20V
- * Standardized, symmetrical output characteris
- * Fully static operation
- * Common reset
- * 5V, 10V, and 15V parametric ratings
- * Noise margin (over full package-tempera ture range):
 - 1V at $V_{DD}=5V$
 - 2V at $V_{DD}=10V$
 - 2.5V at $V_{DD}=15V$

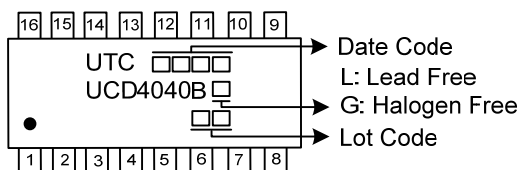


SOP-16

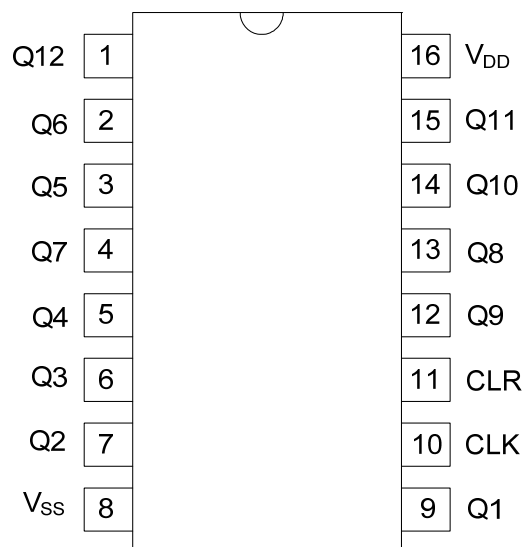
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4040BL-S16-R	UCD4040BG-S16-R	SOP-16	Tape Reel

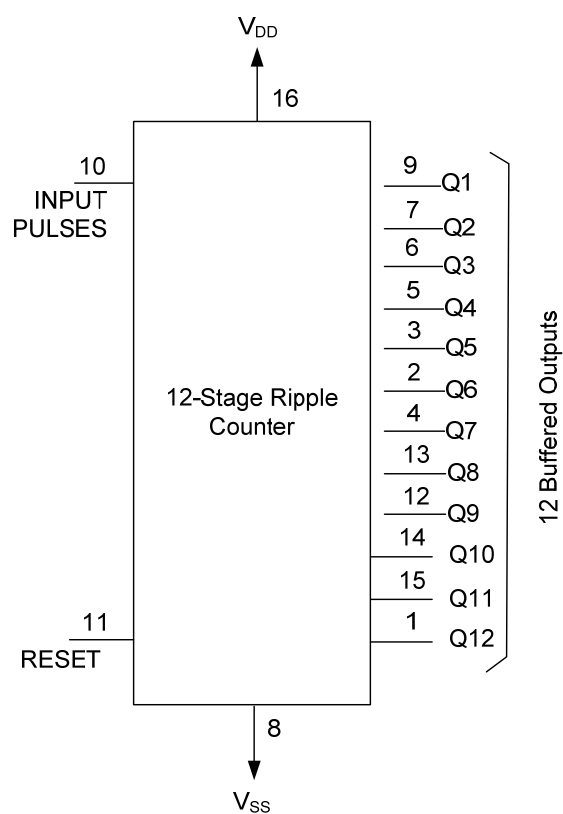
UCD4040BG-S16-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) S16: SOP-16
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

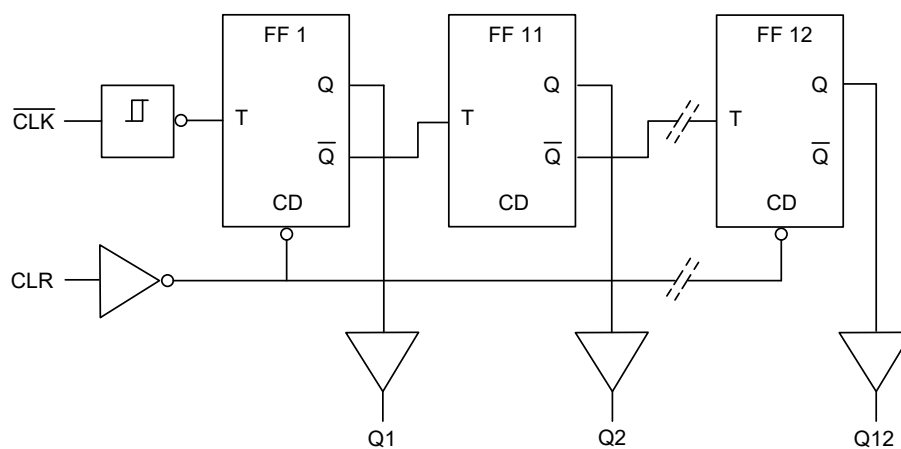
■ PIN CONFIGURATION



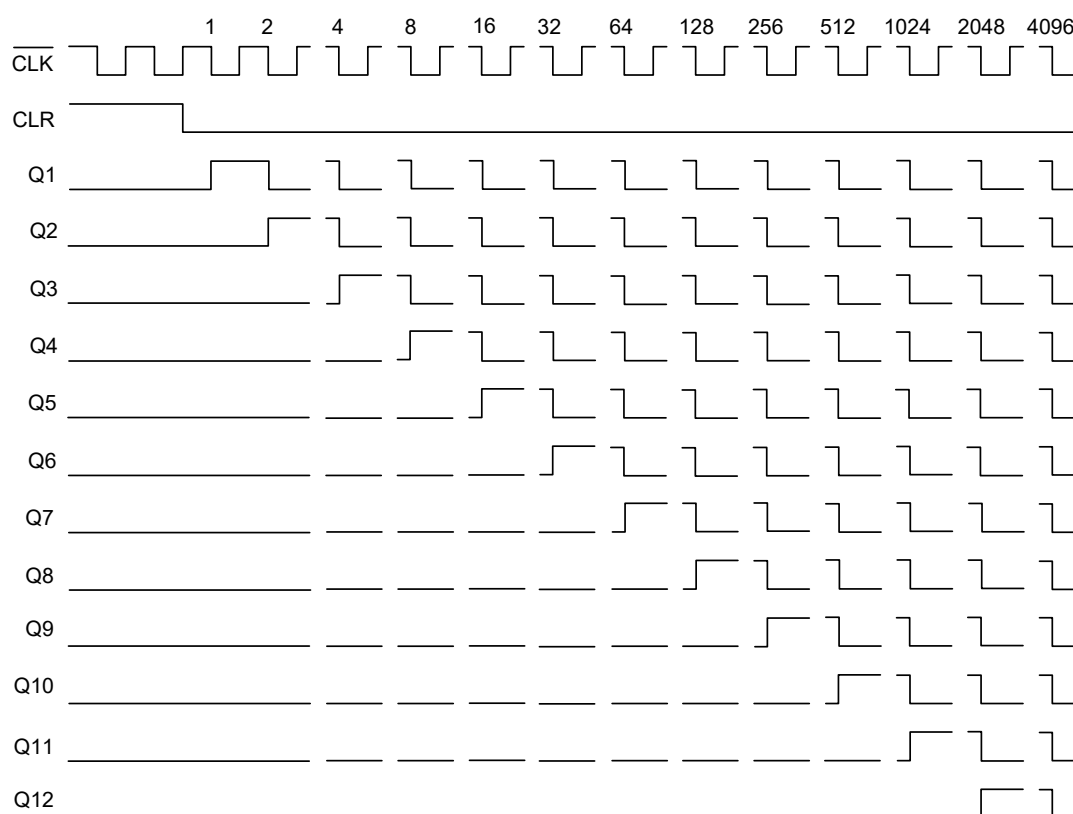
■ FUNCTIONAL DIAGRAM



■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{DD}		-0.5 ~ +18	V
Input Voltage	V_{IN}		-0.5 ~ $V_{DD}+0.5$	V
Continuous Input Current	I_{IN}		±10	mA
Input Clamping Current	I_{IK}	$V_{IN} < -0.5V$ or $V_{IN} > V_{DD}+0.5V$	±10	mA
Output Clamping Current	I_{OK}	$V_{OUT} < -0.5V$ or $V_{OUT} > V_{DD}+0.5V$	±10	mA
Supply Current	I_{DD}		±50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	Operating	3		15	V
Input Voltage	V_{IN}		0		V_{DD}	V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	$V_{DD}=5V, I_{OH} <1\mu A$	4.95			V
		$V_{DD}=10V, I_{OH} <1\mu A$	9.95			V
		$V_{DD}=15V, I_{OH} <1\mu A$	14.95			V
Low-Level Output Voltage	V_{OL}	$V_{DD}=5V, I_{OH} <1\mu A$			0.05	V
		$V_{DD}=10V, I_{OH} <1\mu A$			0.05	V
		$V_{DD}=15V, I_{OH} <1\mu A$			0.05	V
High-Level Input Voltage	V_{IL}	$V_{DD}=5V, V_{OUT}=0.5V$ or $4.5V$			1.5	V
		$V_{DD}=10V, V_{OUT}=1V$ or $9V$			3	V
		$V_{DD}=15V, V_{OUT}=1.5V$ or $13.5V$			4	V
Low-Level Input Voltage	V_{IH}	$V_{DD}=5V, V_{OUT}=0.5V$ or $4.5V$	3.5			V
		$V_{DD}=10V, V_{OUT}=1V$ or $9V$	7			V
		$V_{DD}=15V, V_{OUT}=1.5V$ or $13.5V$	11			V
High-Level Output Current	I_{OH}	$V_{DD}=5V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=2.5V$	-0.51		-1.4	mA
		$V_{DD}=5V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=4.6V$	-1.6		-0.44	mA
		$V_{DD}=10V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=9.5V$	-1.3		-1.1	mA
		$V_{DD}=15V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=13.5V$	-3.4		-3.0	mA
Low-Level Output Current	I_{OL}	$V_{DD}=5V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=0.4V$	0.44		1	mA
		$V_{DD}=10V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=0.5V$	1.1		2.6	mA
		$V_{DD}=15V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=1.5V$	3.0		6.8	mA
Input Leakage Current	$I_{I(LEAK)}$	$V_{DD}=15V$			±0.3	μA
Quiescent Supply Current	I_{DD}	$V_{DD}=5V, I_{OUT}=0A$			20	μA
		$V_{DD}=10V, I_{OUT}=0A$			40	μA
		$V_{DD}=15V, I_{OUT}=0A$			80	μA

Note: I_{OL} and I_{OH} are tested one output at a time.

■ SWITCHING CHARACTERISTICS

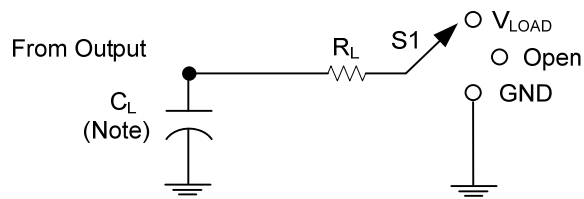
(Input: $t_R=t_F=20\text{ns}$, $C_L=50\text{pF}$, $R_L=200\text{K}\Omega$, $T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (CLK) to Output (Q1)	t_{PHL}/t_{PLH}	$V_{DD}=5\text{V}$			360	ns
		$V_{DD}=10\text{V}$			160	ns
		$V_{DD}=15\text{V}$			130	ns
Propagation Delay From Input (Qn) to Output (Qn+1)	t_{PHL}/t_{PLH}	$V_{DD}=5\text{V}$			330	ns
		$V_{DD}=10\text{V}$			80	ns
		$V_{DD}=15\text{V}$			60	ns
Propagation Delay From Input (CLR) to Output (Qn)	t_{PHL}	$V_{DD}=5\text{V}$			280	ns
		$V_{DD}=10\text{V}$			120	ns
		$V_{DD}=15\text{V}$			100	ns
Output Transition Time	t_{THL}/t_{TLH}	$V_{DD}=5\text{V}$			200	ns
		$V_{DD}=10\text{V}$			100	ns
		$V_{DD}=15\text{V}$			80	ns
Maximum Clock Input Frequency	$f_{\max}$	$V_{DD}=5\text{V}$	3.5			MHz
		$V_{DD}=10\text{V}$	8			MHz
		$V_{DD}=15\text{V}$	12			MHz
Minimum Clock Pulse Width	t_W	$V_{DD}=5\text{V}$	140			ns
		$V_{DD}=10\text{V}$	60			ns
		$V_{DD}=15\text{V}$	40			ns
Minimum Reset Pulse Width	t_W	$V_{DD}=5\text{V}$	200			ns
		$V_{DD}=10\text{V}$	80			ns
		$V_{DD}=15\text{V}$	60			ns
Reset Removal Time	t_{REM}	$V_{DD}=5\text{V}$	350			ns
		$V_{DD}=10\text{V}$	150			ns
		$V_{DD}=15\text{V}$	100			ns

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

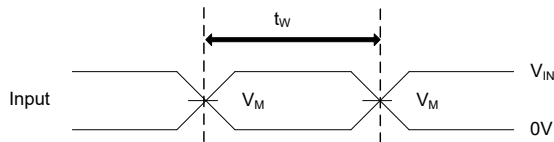
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	Any Input			7.5	pF

■ TEST CIRCUIT AND WAVEFORMS

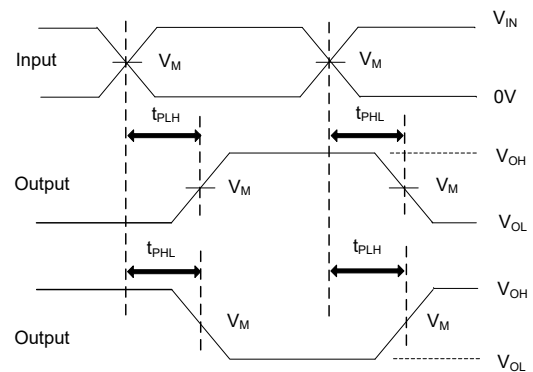


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{DD}	Inputs		V_M	V_{LOAD}	C_L	R_L
	V_{IN}	t_R / t_F				
5V ~ 15V	0 or V_{DD}	$\leq 20\text{ns}$	$0.5 \times V_{DD}$	V_{DD}	50pF	200K Ω



PULSE WIDTH



PROPAGATION DELAY TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 10\text{MHz}$, $Z_0 = 50\Omega$.

■ TEST CIRCUIT AND WAVEFORMS (Cont.)

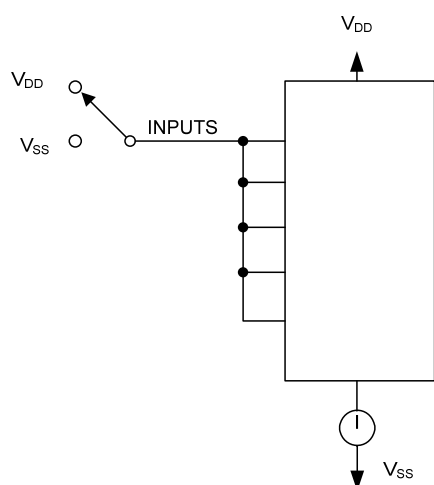


Fig. 1 Quiescent device current test circuit

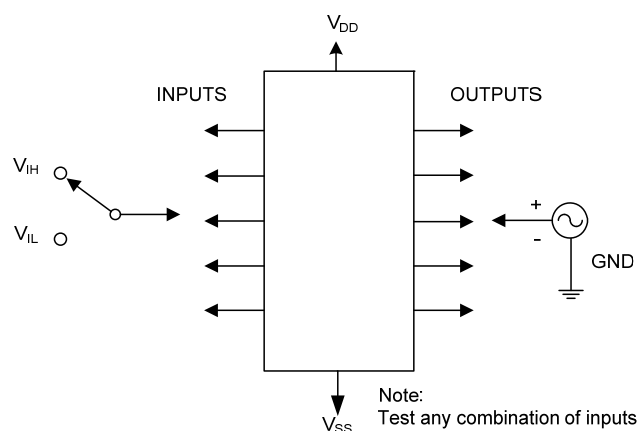


Fig. 2 Input voltage test circuit

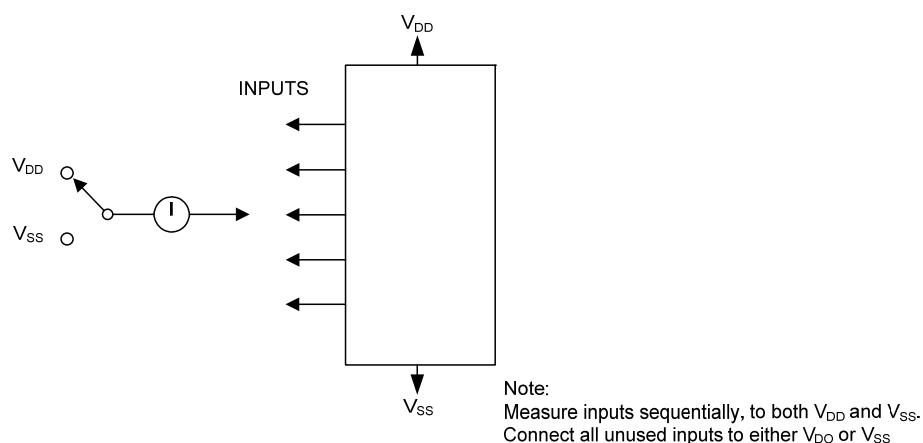


Fig. 3 Input current test circuit

Note: Measure inputs sequentially, to both V_{DD} and V_{SS} ; Connect all unused inputs to either V_{DD} or V_{SS} .

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