



UT3P10M

Preliminary

POWER MOSFET

-3.0A, -100V P-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **UT3P10M** is P-channel enhancement mode Field-Effect Transistor (FET) using Trench MOSFET technology.

It using UTC's are from silicon process technology to achieve the lowest possible on-resistance and fast switching performance. provides the designer with an extreme efficient device for use in a wide range of power applications.

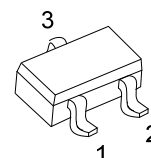
FEATURES

* $R_{DS(ON)} \leq 0.65 \Omega$ @ $V_{GS} = -10V$, $I_D = -3.0A$

$R_{DS(ON)} \leq 0.76 \Omega$ @ $V_{GS} = -4.5V$, $I_D = -1.5A$

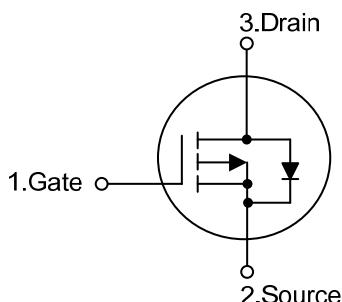
* High Switching Speed

* High Cell Density Trench Technology



SOT-23-3
(JEDEC TO-236)

SYMBOL



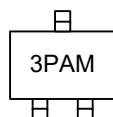
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT3P10ML-AE2-R	UT3P10MG-AE2-R	SOT-23-3	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

UT3P10MG-AE2-R	(1) Packing Type	(1) R: Tape Reel
	(2) Package Type	(2) AE2: SOT-23-3
	(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-3	A
Pulsed Drain Current (Note 2)	I_{DM}	-6	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	8	mJ
Peak Diode Recovery dv/dt	dv/dt	29	V/ns
Power Dissipation	P_D	0.89	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 1\text{mH}$, $I_{AS} = -4\text{A}$, $V_{DD} = -50\text{V}$, $R_G = 25\ \Omega$ Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -3.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	250	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	140	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

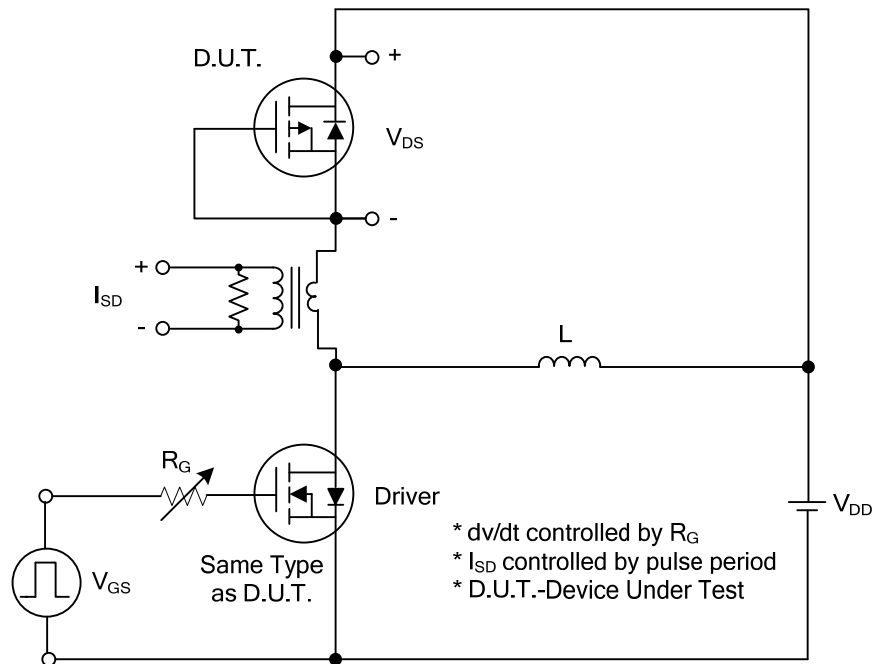
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0 V, I _D =-250μA	-100			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V			-1	μA
Gate-Source Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-3.0A			0.65	Ω
		V _{GS} =-4.5V, I _D =-1.5A			0.76	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =-25V, V _{GS} =0V, f=1.0MHz		502		pF
Output Capacitance	C _{OSS}			28		pF
Reverse Transfer Capacitance	C _{RSS}			19		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =-80V, V _{GS} =-10V, I _D =-3.0A, (Note 1, 2)		15		nC
Gate Source Charge	Q _{GS}			2		nC
Gate Drain Charge	Q _{GD}			3		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =-50V, V _{GS} =-10V, I _D =-3.0A, R _G =6Ω (Note 1, 2)		4		ns
Turn-ON Rise Time	t _r			17		ns
Turn-OFF Delay Time	t _{D(OFF)}			19		ns
Turn-OFF Fall-Time	t _f			19		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				-3	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				-6	A
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-3.0A			-1.4	V
Body Diode Reverse Recovery Time	t _{rr}	V _{GS} = 0V, I _S =-3.0A,		55		ns
Body Diode Reverse Recovery Charge	Q _{rr}	dlf/dt=100A/μs (Note 1)		78		nC

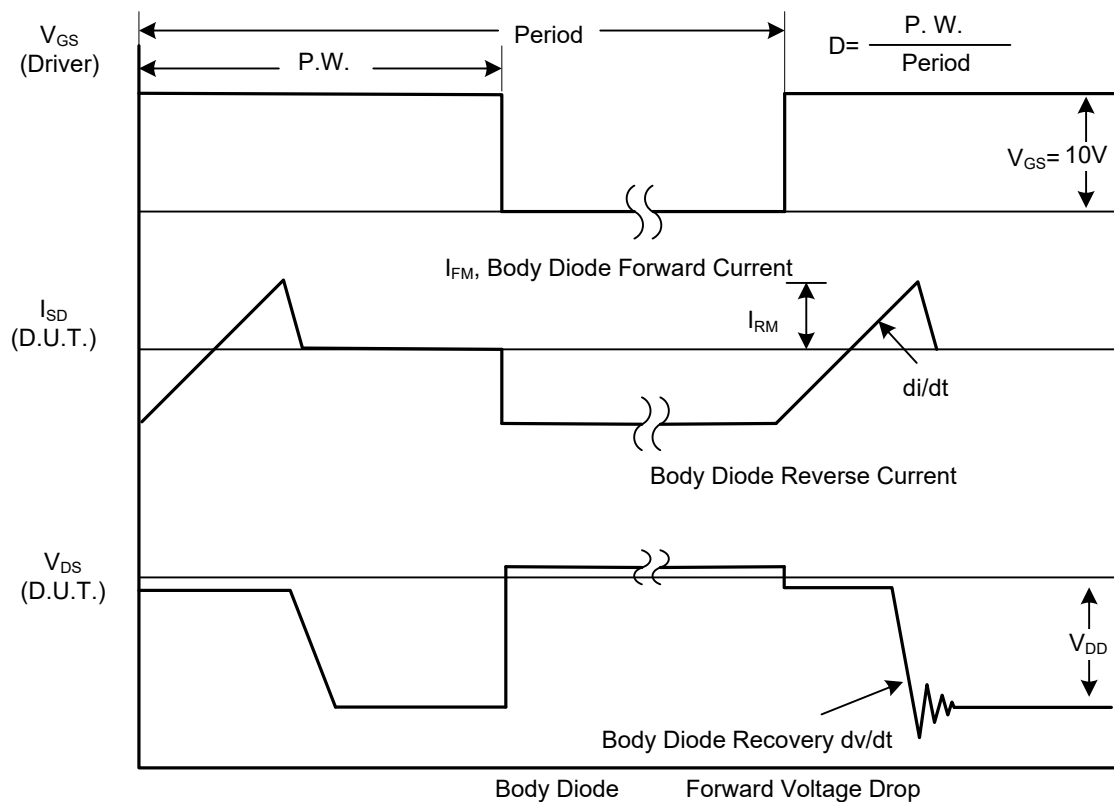
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

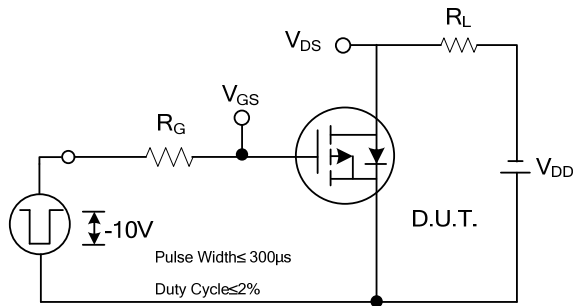


Peak Diode Recovery dv/dt Test Circuit

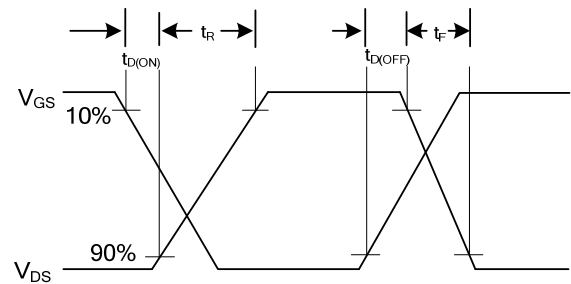


Peak Diode Recovery dv/dt Waveforms

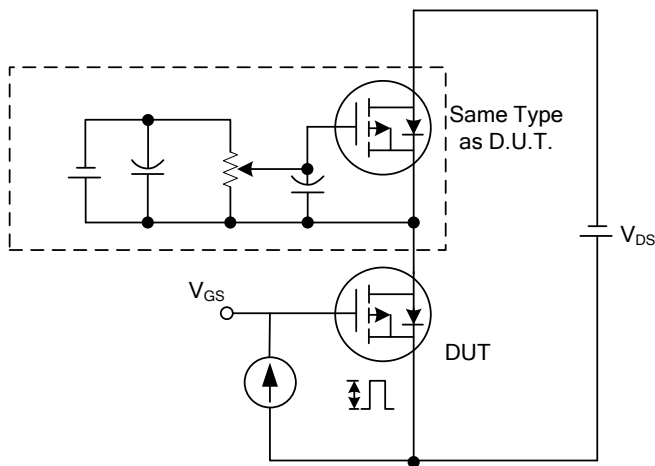
■ TEST CIRCUITS AND WAVEFORMS



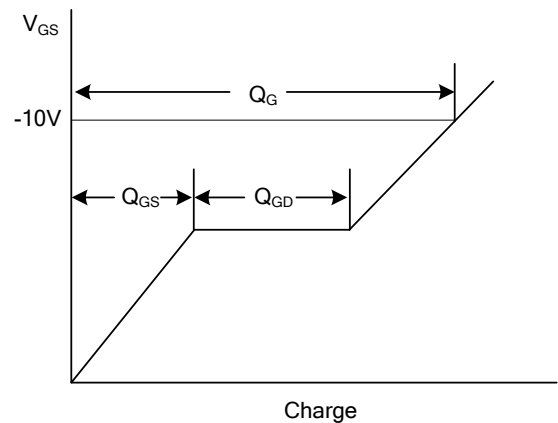
Switching Test Circuit



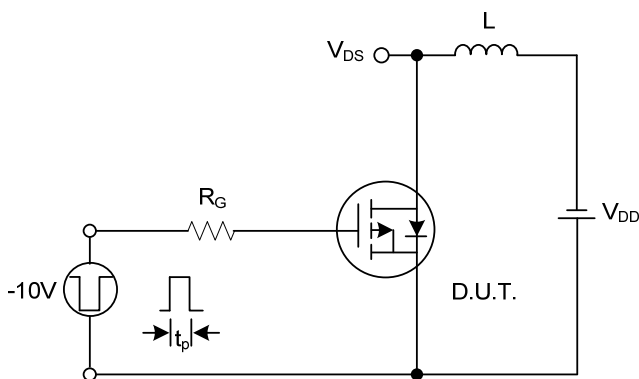
Switching Waveforms



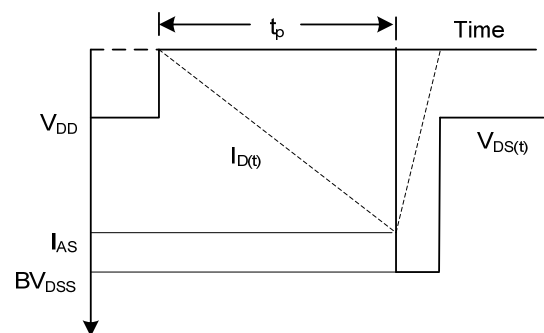
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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