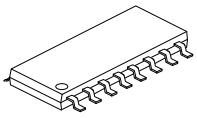
8-BIT PARALLEL-LOAD SHIFT REGISTER



SOP-16

■ DESCRIPTION

The **U74HCT165E** is an 8-bit parallel-load shift register that, when clocked, shifts the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A-H) inputs these are enabled by a low level at shift/load (SH/$\overline{LD}$) input. The **U74HCT165E** also features a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

■ FEATURES

* Complementary Outputs
* Direct Overriding Load (Data) Inputs
* Gated Clock Inputs
* Parallel-to-Serial Data Conversion
* Compatible with TTL, NMOS, CMOS output voltage levels

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT165EL-S16-R	U74HCT165EG-S16-R	SOP-16	Tape Reel

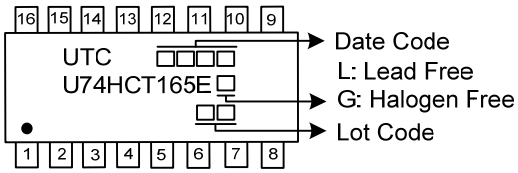
U74HCT165EG-S16-R

(1)Packing Type — (1) R: Tape Reel

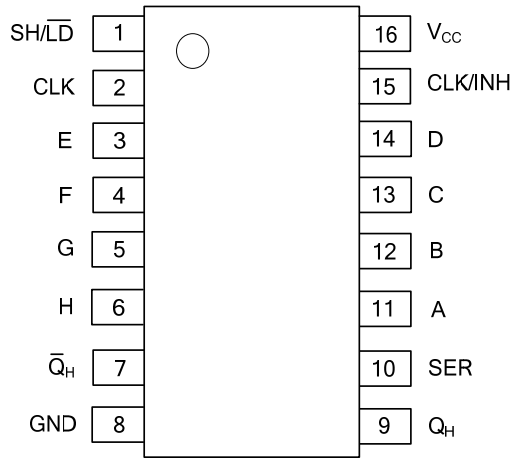
(2)Package Type — (2) S16: SOP-16

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

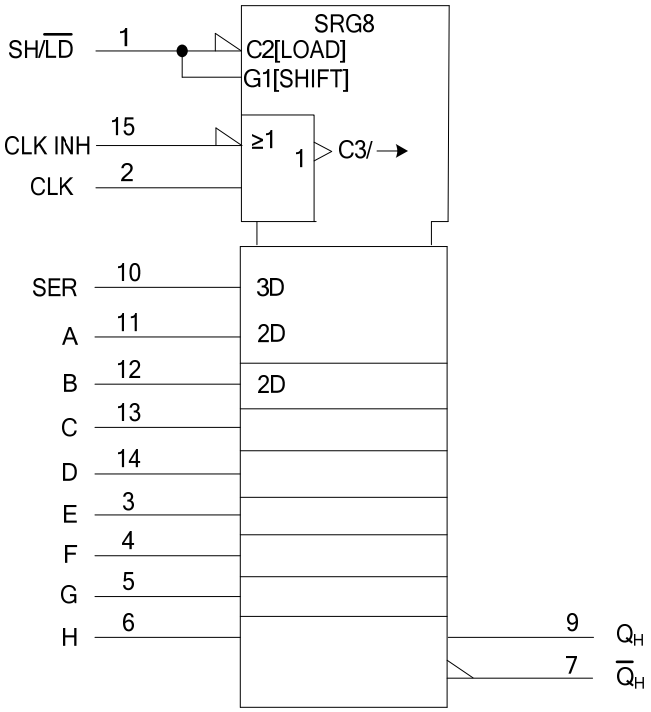


■ FUNCTION TABLE

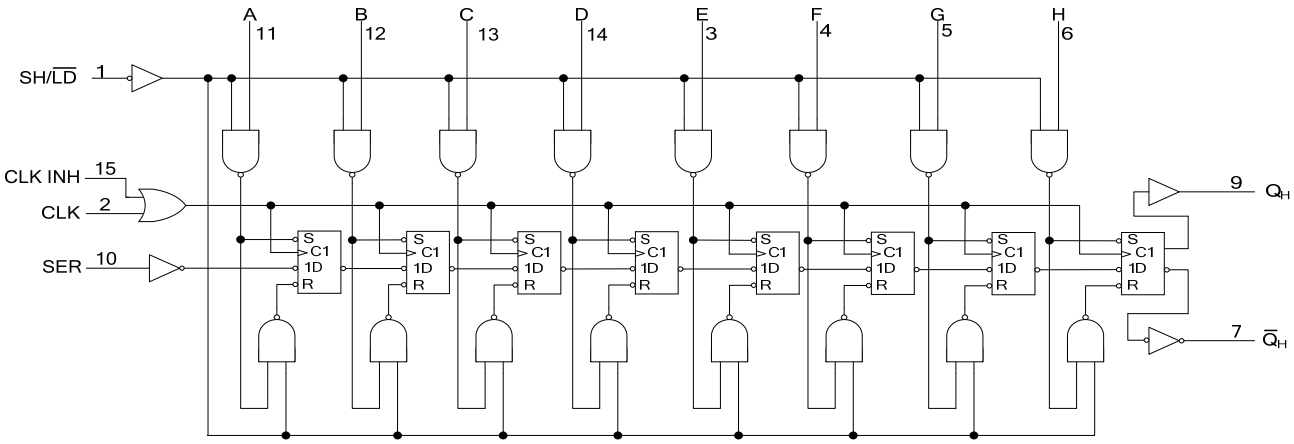
Operating Modes	Inputs					Qn Registers		Outputs	
	SH/$\overline{LD}$	CLK/INH	CLK	SER	A to H	Q_A	Q_B to Q_G	Q_H	$\overline{Q}_H$
Parallel Load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
Serial Shift	H	L	↑	l	X	L	q_A to q_F	q_G	$\overline{q}_G$
	H	L	↑	h	X	H	q_A to q_F	q_G	$\overline{q}_G$
	H	↑	L	l	X	L	q_A to q_F	q_G	$\overline{q}_G$
	H	↑	L	h	X	H	q_A to q_F	q_G	$\overline{q}_G$
Hold “Do Nothing”	H	H	X	X	X	q_A	q_B to q_G	q_H	$\overline{q}_H$
	H	X	H	X	X	q_A	q_B to q_G	q_H	$\overline{q}_H$

Notes: H=HIGH Voltage Level;
h= HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition;
L=LOW Voltage Level;
l= LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition;
q=state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X=don’t care;
↑= LOW-to-HIGH clock transition.

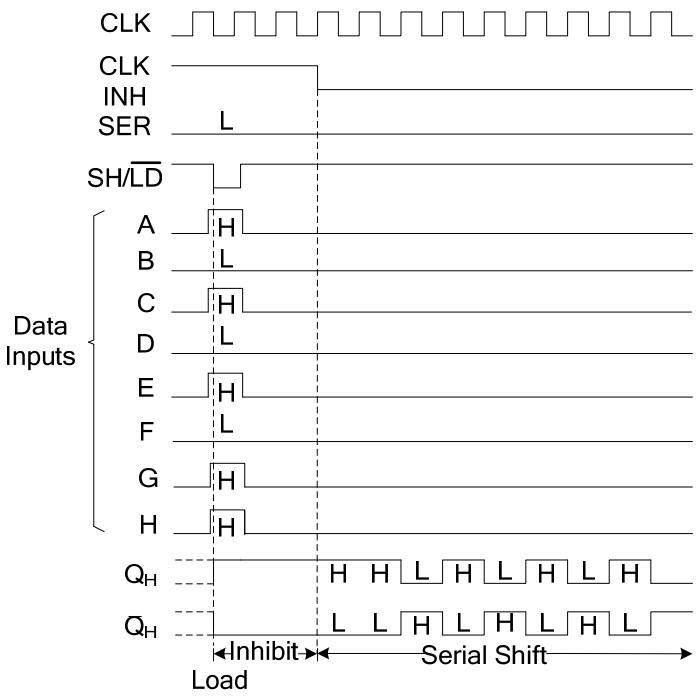
■ LOGIC SYMBOL



■ LOGIC DIAGRAM (positive logic)



■ TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCE



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7	V
V_{CC} or GND Current	I_{CC}		±50	mA
Output Current	I_{OUT}	V_{OUT}= 0 to V_{CC}	±25	mA
Input Clamp Current	I_{IK}	V_{IN}<0 or V_{IN}>V_{CC}+0.5V	±20	mA
Output Clamp Current	I_{OK}	V_{OUT}<0 or V_{OUT}>V_{CC}+0.5V	±20	mA
Electrostatic Discharge	$V_{(ESD)}$	Human-Body Model (HBM) Per JESD22-A114/115	2000	V
Storage Temperature	T_{STG}		-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Time	t_R / t_F	V_{CC}=4.5V~5.5V			500	ns
Operating Free-air Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	73	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=4.5V~5.5V	2			V
Low-Level Input Voltage	V_{IL}	V_{CC}=4.5V~5.5V			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.5		V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.28		V
Low-Level Output Voltage	V_{OL}	V_{CC}=4.5V, I_{OL}=20μA		0	0.1	V
		V_{CC}=4.5V, I_{OL}=4mA		0.15	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}= V_{CC} or GND			±100	nA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND			8	μA
Additional supply current	$\triangle I_{CC}$	V_{IN}=V_{CC}-2.1V,other inputs at V_{CC} or GND,V_{CC}=4.5V to 5.5V, DS, Dn inputs			126	uA
		V_{IN}=V_{CC}-2.1V, other inputs at V_{CC} or GND, V_{CC}=4.5V to 5.5V, CLK,CLKINH,SH/$\overline{LD}$ inputs			234	uA
Input Capacitance	C_I				10	pF

■ TIMING REQUIREMENTS (T_A =25°C , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency		f_{CLOCK}	V_{CC}=4.5V	26			MHz
Pulse duration	CLK high input	t_W	V_{CC}=4.5V	18			ns
	SH/$\overline{LD}$ low input		V_{CC}=4.5V	20			ns
Setup time	DS before CLK,CLK INH	t_{SU}	V_{CC}=4.5V	20			ns
	CLK INH to CLK, CLK to CLK INH		V_{CC}=4.5V	20			ns
	Dn to SH/$\overline{LD}$		V_{CC}=4.5V	20			ns
Hold time	DS to CLK，CLK INH	t_H	V_{CC}=4.5V	7			ns
	CLK to CLK INH，CLK INH to CLK		V_{CC}=4.5V	7			ns

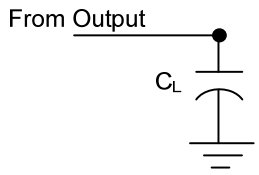
■ SWITCHING CHARACTERISTICS (t_R = t_F= 6ns, C_L=50pF, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from SH/$\overline{LD}$ to QH or $\overline{Q}_H$	t_{PD} (t_{PLH}/ t_{PHL})	V_{CC}=4.5V			40	ns
		V_{CC}=5V, C_L=15pF		17	40	ns
Propagation delay from CLK, CLK, INH to QH or $\overline{Q}_H$		V_{CC}=4.5V			40	ns
		V_{CC}=5V, C_L=15pF		14	40	ns
Propagation delay from D7 to QH or $\overline{Q}_H$		V_{CC}=4.5V			35	ns
		V_{CC}=5V, C_L=15pF		11	35	ns
Transition time	t_T	V_{CC}=4.5V		~~7~~	15	ns

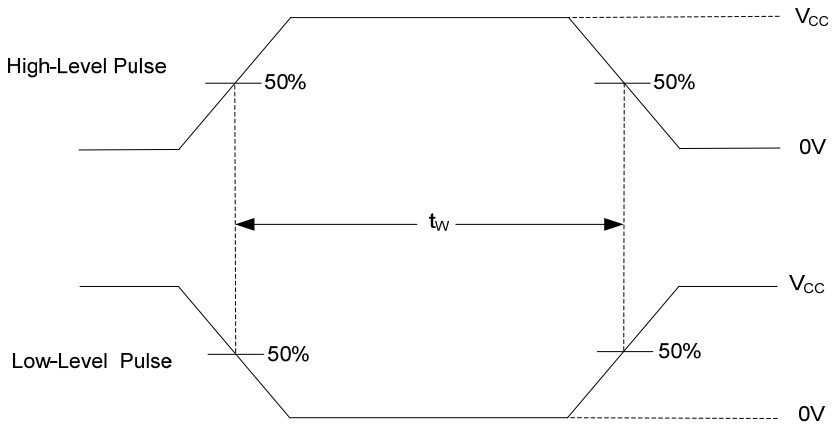
■ OPERATING CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		35		pF

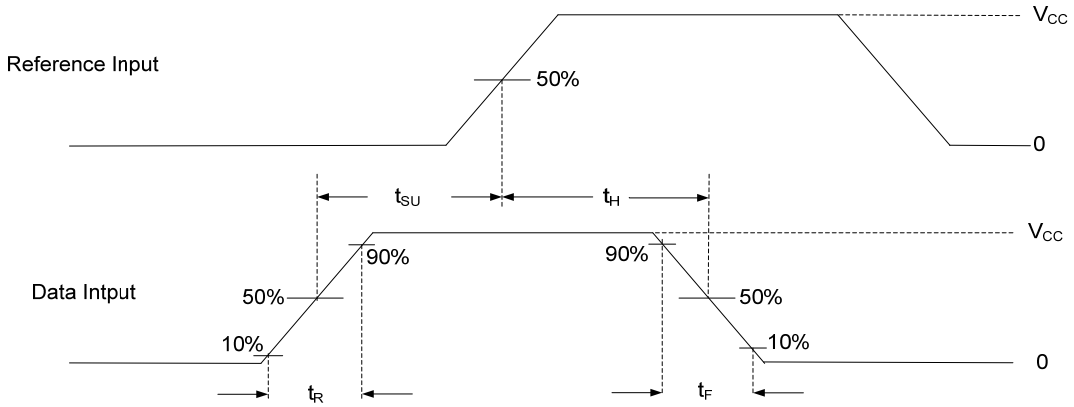
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

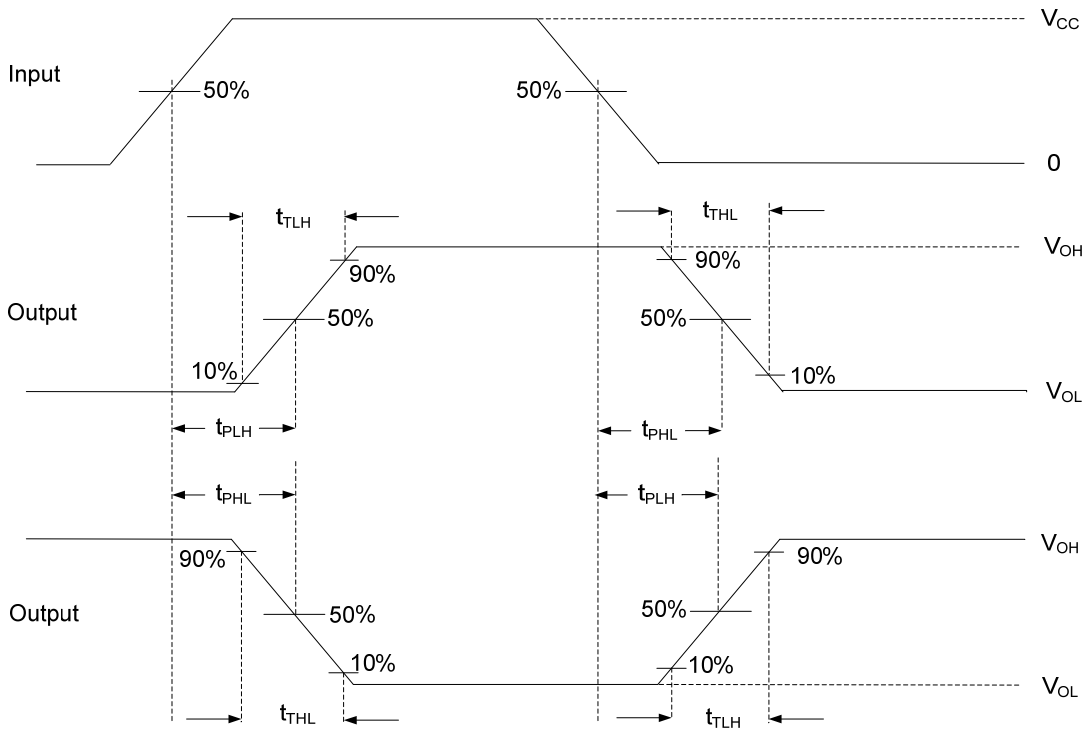


PULSE DURATIONS



SET AND HOLD AND INPUT RISE AND FALL TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Note : t_{THL} and t_{TLH} are the same as t_T