



UT4P10M

Preliminary

POWER MOSFET

-4.0A, -100V P-CHANNEL POWER MOSFET

DESCRIPTION

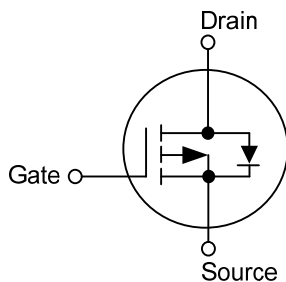
The UTC **UT4P10M** is a P-channel MOS Field Effect Transistor. it uses UTC's advanced technology to provide the customers with high switching speed and a minimum on-state resistance.

The UTC **UT4P10M** is suitable for high voltage switching applications.

FEATURES

- * $R_{DS(ON)} \leq 500 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -2.0\text{A}$
- * $R_{DS(ON)} \leq 600 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -2.0\text{A}$
- * High switching speed
- * Low input capacitance

SYMBOL



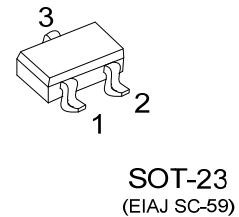
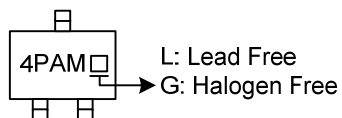
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT4P10ML-AE3-R	UT4P10MG-AE3-R	SOT-23	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

UT4P10MG-AE3-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) AE3: SOT-23
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-100	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	DC	I_D	-4	A
	Pulsed (Note 2)	I_{DM}	-12	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	6.7	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.25	V/ns
Power Dissipation ($T_A=25^{\circ}\text{C}$)		P_D	0.3	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = -11.6\text{A}$, $V_{DD} = -70\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -4.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	416	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

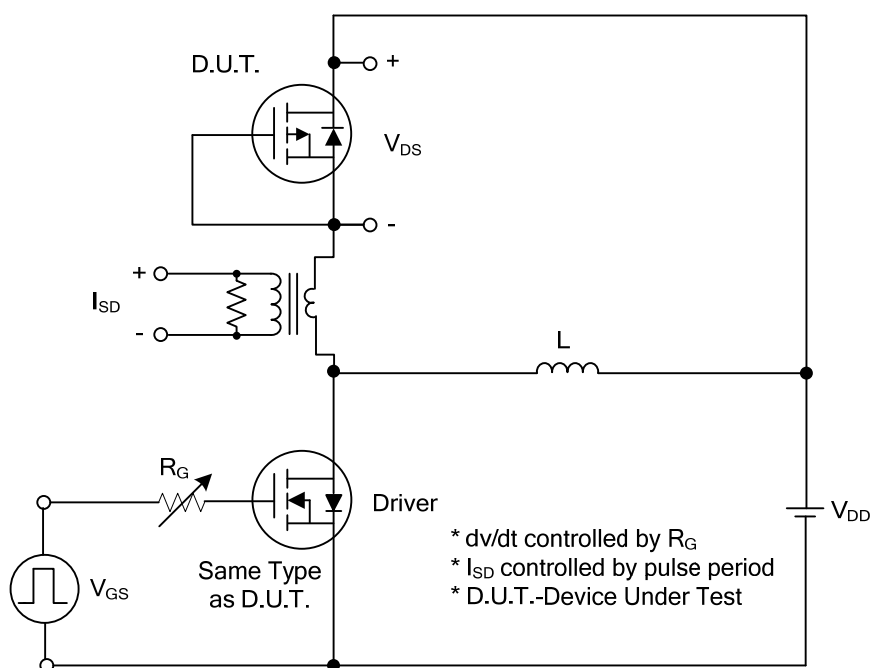
■ ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =-250μA	-100			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-100V, V _{GS} =0V			-1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note 1, 2)		R _{DS(ON)}	V _{GS} =-10V, I _D =-2.0A			500	mΩ
			V _{GS} =-4.5V, I _D =-2.0A			600	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		680		pF
Output Capacitance		C _{OSS}			35		pF
Reverse Transfer Capacitance		C _{RSS}			25		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =-80V, V _{GS} =-10V, I _D =-4.0A, (Note 1, 2)		18		nC
Gate to Source Charge		Q _{GS}			2		nC
Gate to Drain Charge		Q _{GD}			4		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DS} =-50V, V _{GS} =-10V, I _D =-4.0A, R _G =3Ω (Note 1, 2)		6		ns
Rise Time		t _R			18		ns
Turn-OFF Delay Time		t _{D(OFF)}			19		ns
Fall-Time		t _F			19		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S	(Note 1, 2)			-4	A
Diode Forward Voltage		V _{SD}	I _F =-4.0A, V _{GS} =0V (Note 1, 2)			-1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _F =-4.0A, V _{GS} =0V, di/dt=100A/μs		37		ns
Body Diode Reverse Recovery Charge		Q _{rr}			61		nC

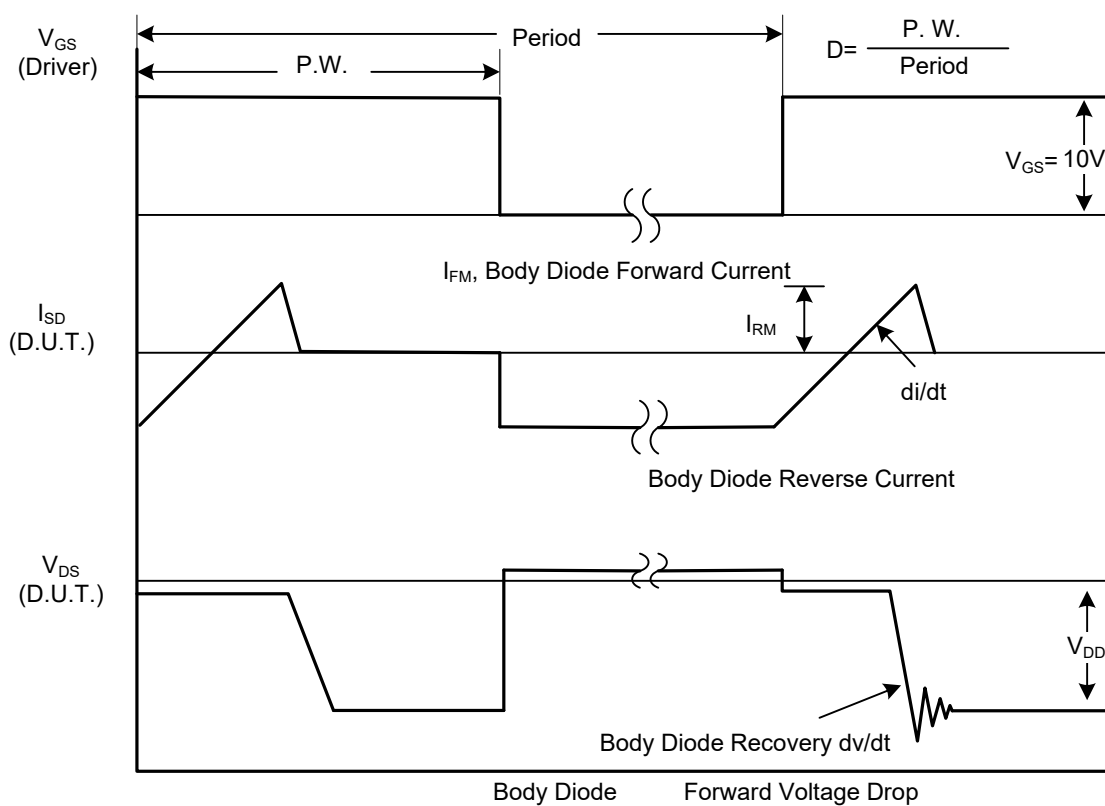
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

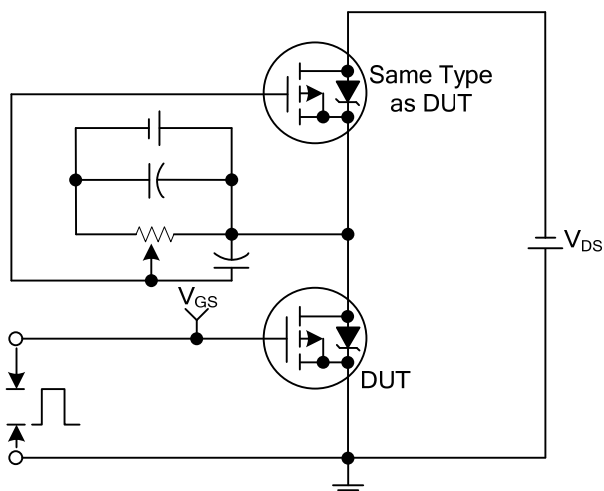


Peak Diode Recovery dv/dt Test Circuit

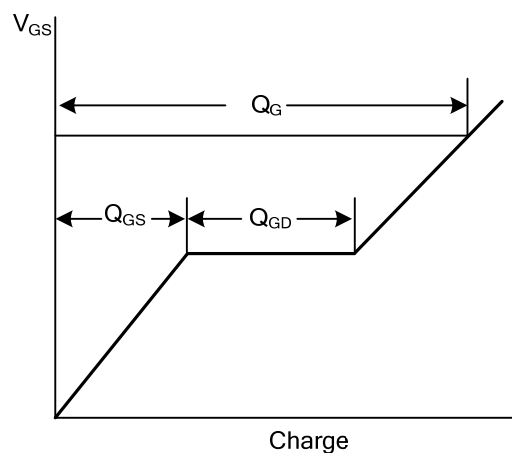


Peak Diode Recovery dv/dt Waveforms

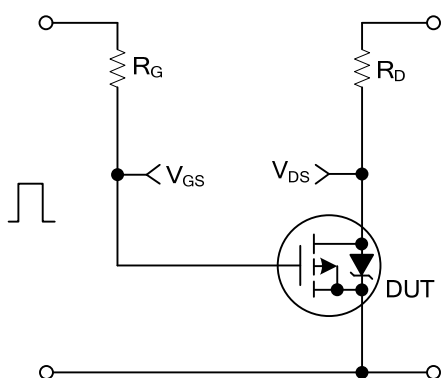
■ TEST CIRCUITS AND WAVEFORMS



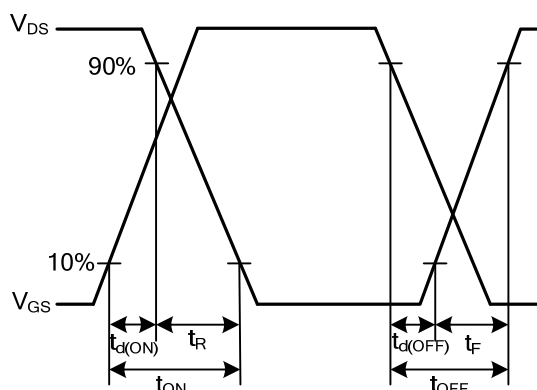
Gate Charge Test Circuit



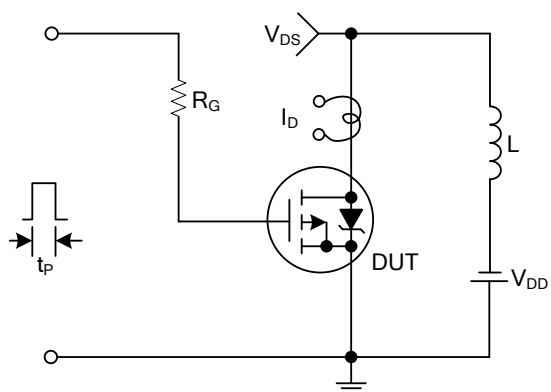
Gate Charge Waveforms



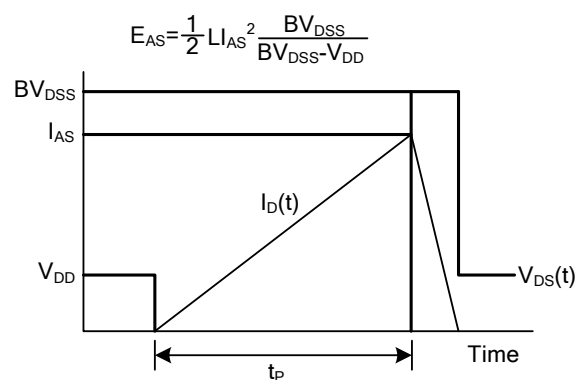
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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