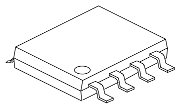
3.0W AUDIO POWER AMPLIFIER WITH ACTIVE-HIGH SHUTDOWN MODE



SOP-8

■ DESCRIPTION

The UTC **PA7382** is a Class-AB audio power amplifier. As a power amplifier which is operating on a single 5V supply, the UTC **PA7382** is capable of delivering 3.0W of output power into 3Ω BTL load with less than 10% distortion.

The UTC **PA7382** does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The UTC **PA7382** features a low-power consumption shutdown mode. The UTC **PA7382** contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions. The UTC **PA7382** is unity-gain stable and can be configured by external gain-setting resistors.

■ FEATURES

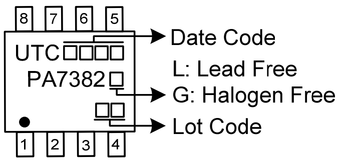
* Operating voltage: 2.2 ~ 5.5V
* Power Output at 5.0V, 10% THD+N, 3Ω 3.0W (Typ.)
* Power Output at 5.0V, 10% THD+N, 4Ω 2.5W (Typ.)
* Power Output at 5.0V, 10% THD+N, 8Ω 1.5W (Typ.)
* Shutdown Current 0.6μA (Typ.)
* No output coupling capacitors, snubber networks or bootstrap capacitors required
* External gain configuration capability
* Shutdown mode when a high level is applied on shutdown

■ ORDERING INFORMATION

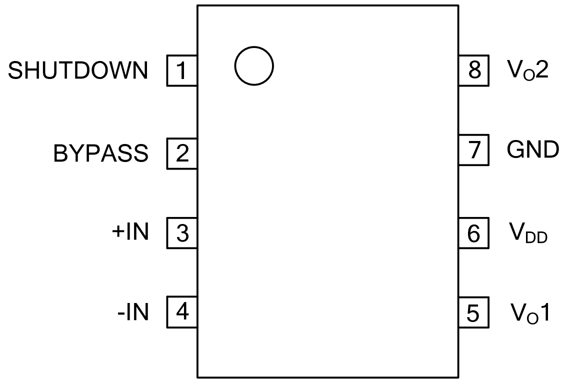
Ordering Number		Package	Packing
Lead Free	Halogen Free		
PA7382L-S08-R	PA7382G-S08-R	SOP-8	Tape Reel

PA7382G-S08-R	
(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) S08: SOP-8
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



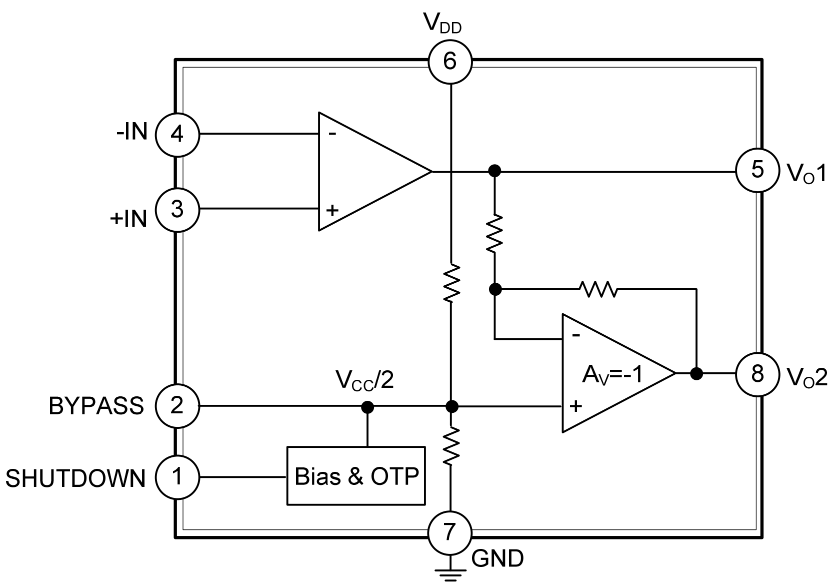
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	SHUTDOWN	Shutdown control input pin. The device enters in shutdown mode when a high level is applied on this pin.
2	BYPASS	Connected to a bypass capacitor.
3	+IN	Positive input
4	-IN	Negative input
5	V_O1	Negative output
6	V_{DD}	Supply voltage
7	GND	Ground
8	V_O2	Positive output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6	V
Input Voltage	V_{IN}	GND ~ V_{DD}	V
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	220	°C/W
Junction to Case	θ_{JC}	60	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{DD}=5V, f=1kHz, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Power Supply Current	I_{DD}	V_{IN}=0V, I_O=0A, No load		3.5	10	mA
Shutdown Current	I_{OFF}	V_{PIN1}=V_{CC}		0.6		µA
Output Offset Voltage	V_{OS}	V_{IN}=0V		8.0	50	mV
Output Power	P_O	THD=1%, f=1kHz, R_L=8Ω		1.2		W
		THD=1%, f=1kHz, R_L=4Ω		2.0		W
		THD=1%, f=1kHz, R_L=3Ω		2.4		W
		THD=10%, f=1kHz, R_L=8Ω		1.5		W
		THD=10%, f=1kHz,R_L=4Ω		2.5		W
		THD=10%, f=1kHz,R_L=3Ω		3.0		W
Minimum Harmonic Distortion	THD	f=1kHz, R_L=8Ω, P_O=1W		0.15		%
		f=1kHz, R_L=3Ω, P_O=2W		0.3		%
Power Supply Rejection Ratio	PSRR	V_{CC}=4.9V ~ 5.1V		60		dB

■ TYPICAL APPLICATION CIRCUIT

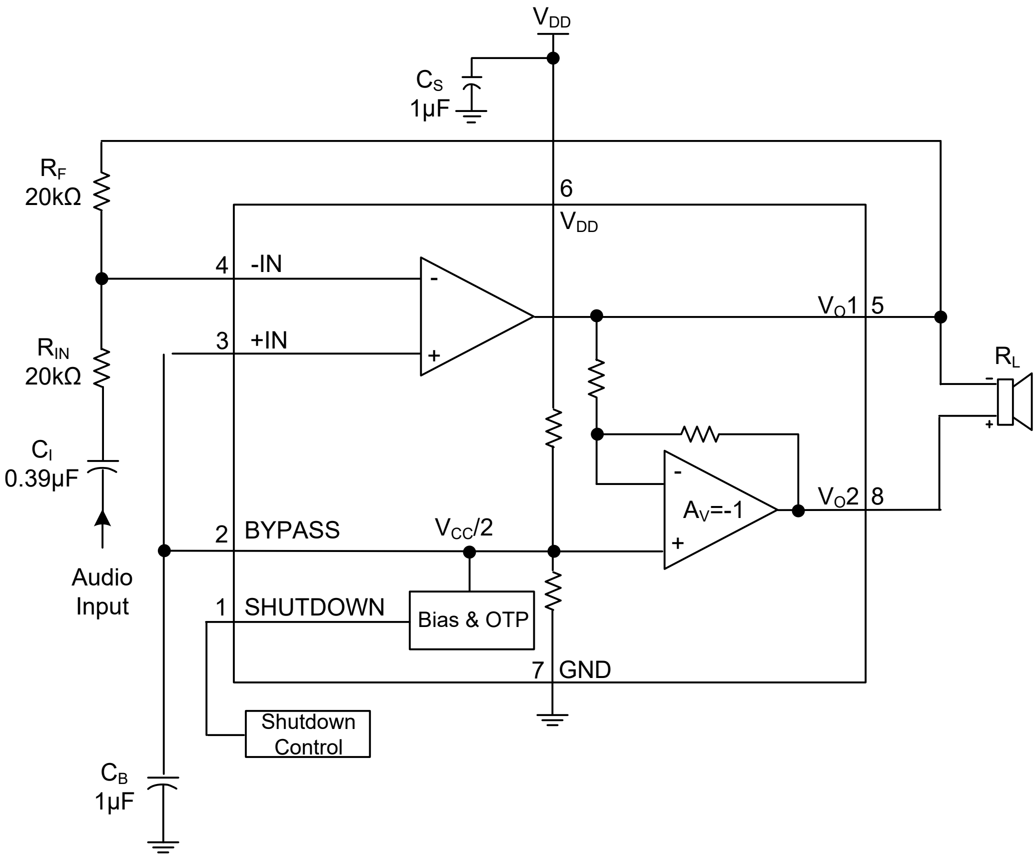


Fig 1. Typical Application Schematic

■ TYPICAL APPLICATION CIRCUIT (Cont.)

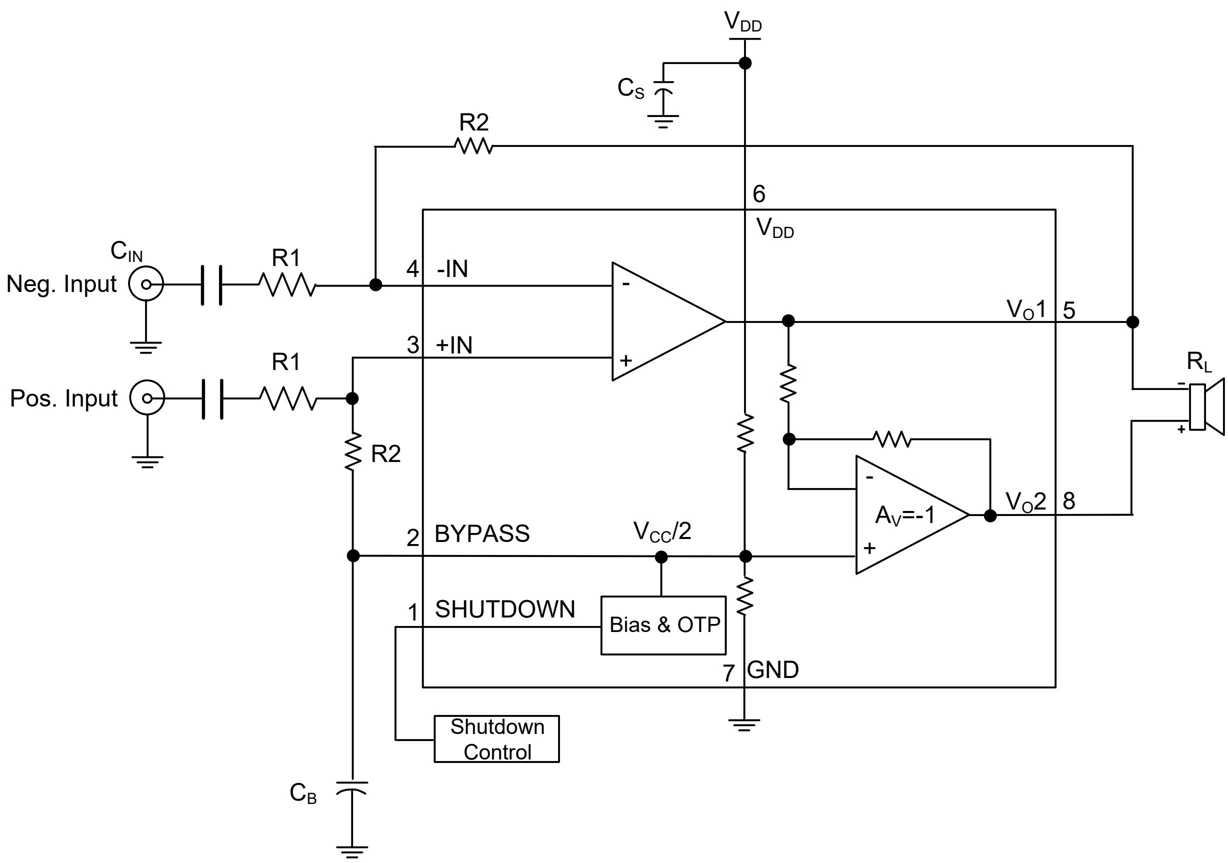


Fig 2. Differential Input Amplifier Configuration

■ BRIDGE CONFIGURATION EXPLANATION

The **PA7382** has two internal operational amplifiers as shown in the Figure 1. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_F to R_{IN}. In the Figure 1, the output of first amplifier ~~one~~ serves as the input to second amplifier ~~two~~ which results in both amplifiers generating signals identical in magnitude, but out of phase by 180°. The differential gain for the IC is

$$A_{VD}=2\times\frac{R_F}{R_{IN}}$$

■ SELECTION OF INPUT CAPACITOR SIZE

The click and pop performance is affected by the size of the input coupling capacitor C_{IN}. This charge comes from the output via the feedback and is apt to create pops upon device enable. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 VDD).Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

In addition to minimizing the input capacitor size, the bypass capacitor value is be also considered carefully. Bypass capacitor C_B, is the most critical component to minimize turn-on pops because it determines how fast the **PA7382** turns on. The slower the **PA7382**'s outputs ramp to their quiescent DC voltage (nominally 1/2 VDD), the smaller the turn-on pop. The device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, but it will be much more susceptible to turn-on clicks and pops. Choosing C_B equal to 1.0µF along with a small value of C_{IN} (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. Thus, a value of C_B equal to 1.0µF is recommended only if the most cost sensitive designs.

■ AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output:	1Wrms
Load Impedance:	8Ω
Input Level:	1Vrms
Input Impedance:	20kΩ
Bandwidth:	100Hz-20kHz ±0.25Db

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the **PA7382** to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions in the power dissipation.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation.

$$A_{VD}\geq\frac{\sqrt{(P_O R_L)}}{V_{IN}}=\frac{V_{ORMS}}{V_{INRMS}}$$

$$\frac{R_F}{R_{IN}}=\frac{A_{VD}}{2}$$

From Equation, the minimum A_{VD} is 2.83; use A_{VD} =3. Since the desired input impedance was 20kΩ, and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_F to R_{IN} results in an allocation of R_{IN}=20kΩ and R_F=30kΩ. The final design step is to make sure the bandwidth requirements which must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

$$f_L=\frac{100Hz}{5}=20Hz$$

$$f_H=20kHz\times5=100kHZ$$

■ AUDIO POWER AMPLIFIER DESIGN (Cont.)

R_{IN} in conjunction with C_{IN} create a highpass filter.

$$C_{IN} \geq \frac{1}{2\pi \times 20k\Omega \times 20Hz} = 0.397\mu F$$

Use 0.39µF. The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD}=3 and f_H= 100kHz, the resulting GBWP=300kHz which is much smaller than the **PA7382** GBWP of 2.5MHz. The above description displays that if a designer has a need to design an amplifier with a higher differential gain, the **PA7382** can still be used without running into bandwidth limitations.