



1.0A, 40V N-CHANNEL LOGIC LEVEL ENHANCEMENT MODE

DESCRIPTION

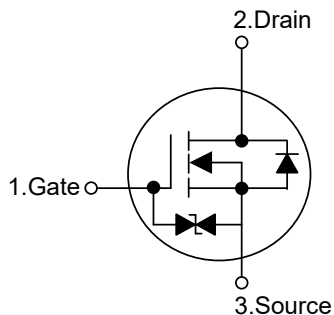
The UTC **UT1N04VZ** employs advanced MOSFET technology and features low gate charge while maintaining low on-resistance.

Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

FEATURES

- * $R_{DS(ON)} \leq 230 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=1.0\text{A}$
- $R_{DS(ON)} \leq 250 \text{ m}\Omega$ @ $V_{GS} = 4.5\text{V}$, $I_D = 0.5\text{A}$
- $R_{DS(ON)} \leq 350 \text{ m}\Omega$ @ $V_{GS} = 2.5\text{V}$, $I_D = 0.3\text{A}$
- * Low Capacitance
- * Low Gate Charge

SYMBOL

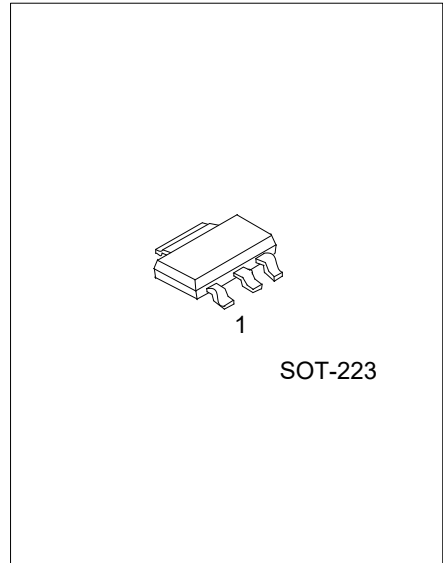


ORDERING INFORMATION

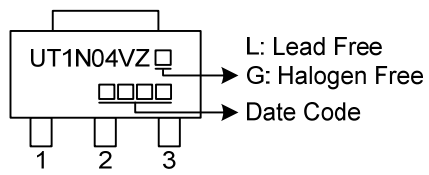
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT1N04VZL-AA3-R	UT1N04VZG-AA3-R	SOT-223	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT1N04VZG-AA3-R (1) Packing Type (2) Package Type (3) Green Package		(1) R: Tape Reel (2) AA3: SOT-223 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 10	V
Continuous Drain Current	I_D	1	A
Pulsed Drain Current (Note 2)	I_{DM}	2	A
Avalanche Energy	E_{AS}	0.87	mJ
Single Pulsed			
Peak Diode Recovery dv/dt (Note 4)	dv/dt	2.65	V/ns
Power Dissipation	P_D	1.1	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. $L = 0.1\text{mH}$, $I_{AS} = 4.2\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\Omega$ Starting $T_J = 25^{\circ}\text{C}$
4. $I_{SD} \leq 1.0\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	125	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	114	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

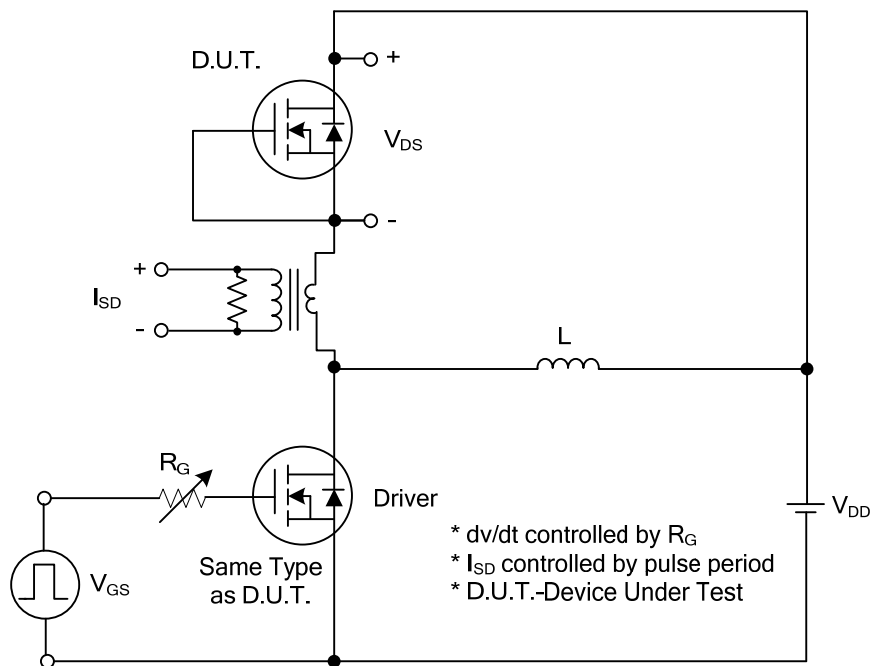
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+10V, V _{DS} =0V			10	μA
	Reverse		V _{GS} =-10V, V _{DS} =0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D =250μA	0.5		1.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A			230	mΩ
			V _{GS} =4.5V, I _D =0.5A			250	mΩ
			V _{GS} =2.5V, I _D =0.3A			350	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1MHz		87		pF
Output Capacitance		C _{OSS}			16		pF
Reverse Transfer Capacitance		C _{RSS}			10		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DD} =32V, V _{GS} =10V, I _D =1.0A (Note 1, 2)		11		nC
Gate to Source Charge		Q _{GS}			1.9		nC
Gate to Drain Charge		Q _{GD}			1.8		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =20V, V _{GS} =10V, I _D =1.0A, R _G =3.3Ω (Note 1, 2)		8		ns
Rise Time		t _R			21		ns
Turn-OFF Delay Time		t _{D(OFF)}			191		ns
Fall-Time		t _F			75		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				1	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				2	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =1.0A, V _{GS} =0V			1	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =1.0A, V _{GS} =0V, dI _F /dt=100A/μs		65		nS
Body Diode Reverse Recovery Charge		Q _{rr}			84		nC

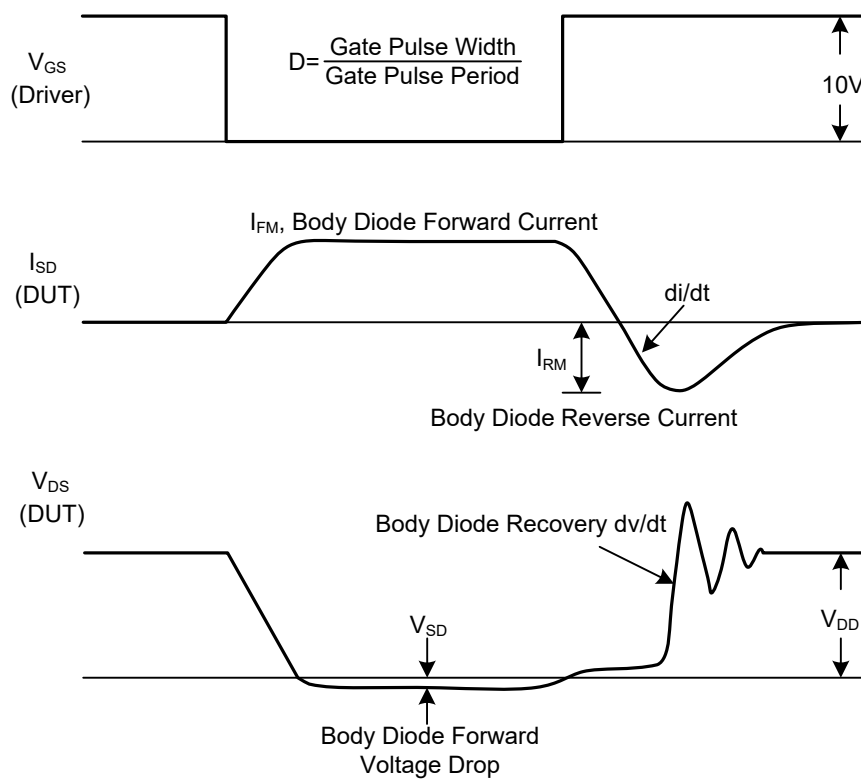
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

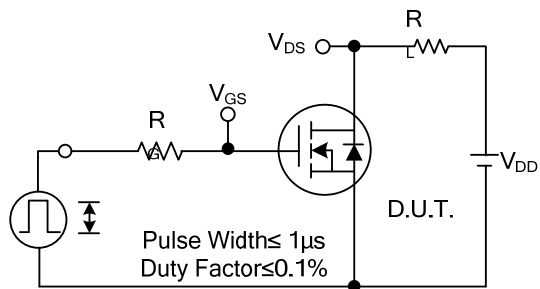


Peak Diode Recovery dv/dt Test Circuit

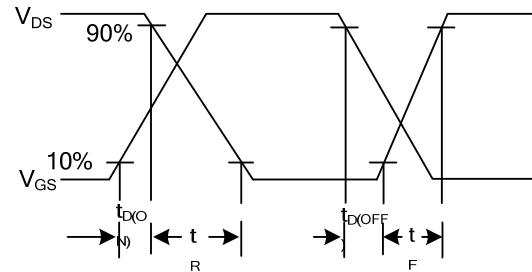


Peak Diode Recovery dv/dt Waveforms

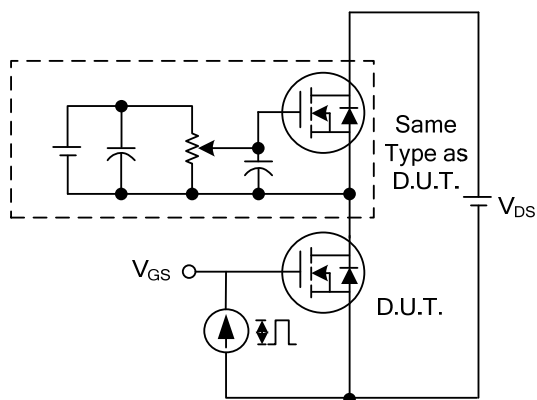
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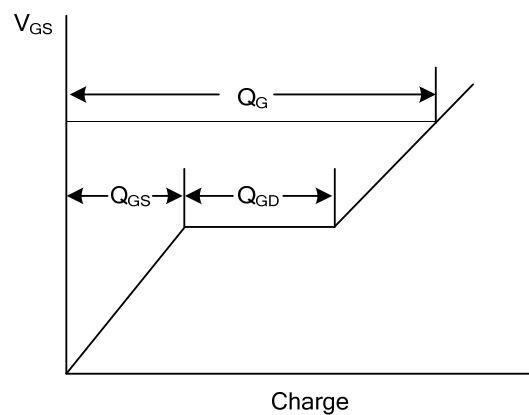
Switching Test Circuit



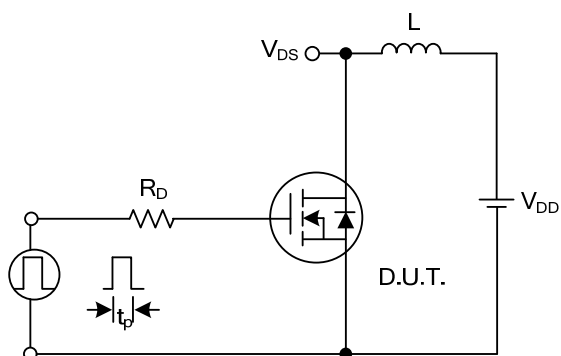
Switching Waveforms



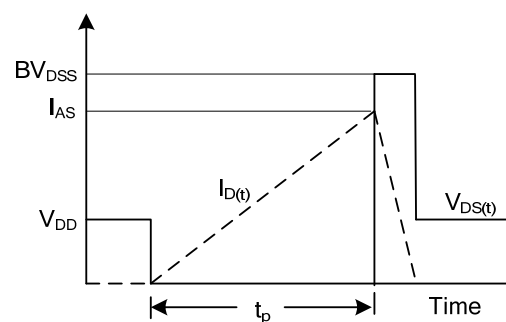
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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