



2NK120QZ

Preliminary

POWER MOSFET

2.0A, 1200V N-CHANNEL POWER MOSFET

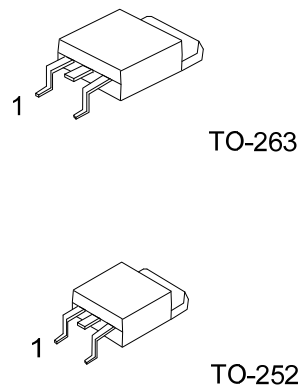
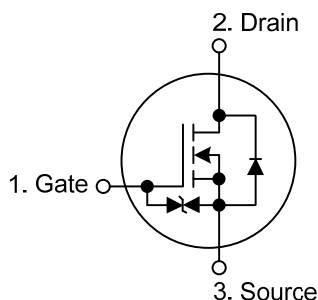
DESCRIPTION

The UTC **2NK120QZ** is a silicon N-channel MOSFET, it uses UTC's advanced technology to provide the customers with a minimum on state resistance, high switching speed and low gate charge.

FEATURES

- * $R_{DS(ON)} \leq 9.6 \Omega$ @ $V_{GS}=10V$, $I_D=1.0A$
- * High switching speed
- * Low input capacitance
- * With ESD protection

SYMBOL



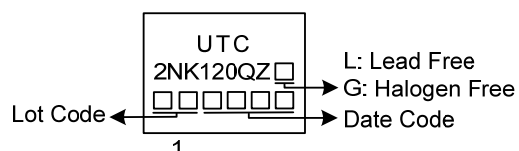
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2NK120QZL-TN3-R	2NK120QZG-TN3-R	TO-252	G	D	S	Tape Reel
2NK120QZL-TQ2-T	2NK120QZG-TQ2-T	TO-263	G	D	S	Tube
2NK120QZL-TQ2-R	2NK120QZG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

2NK120QZG-TN3-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel, T: Tube (2) TN3: TO-252, TQ2: TO-263 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	1200	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	DC	I_D	2	A
	Pulsed (Note 2)	I_{DM}	6	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	63	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	5.9	V/ns
Power Dissipation	TO-252	P_D	50	W
	TO-263		66	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 100\text{mH}$, $I_{AS} = 1.125\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
	TO-263		62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-252	θ_{JC}	2.5 (Note)	$^{\circ}\text{C}/\text{W}$
	TO-263		1.89 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

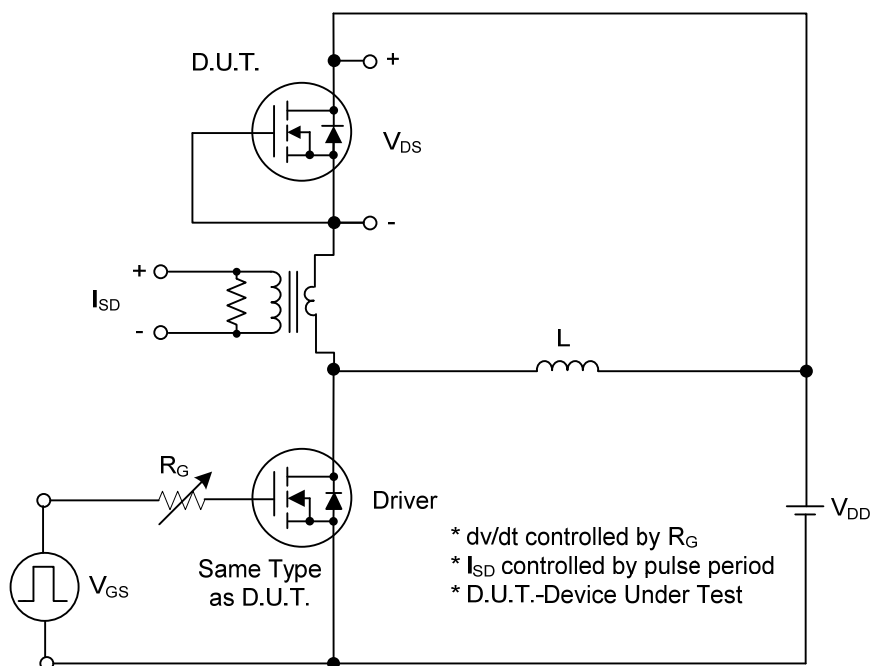
■ ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	1200			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =1200V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+10	μA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	3.0		5.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A		8.0	9.6	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		634		pF
Output Capacitance		C _{OSS}			44		pF
Reverse Transfer Capacitance		C _{RSS}			4.5		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =960V, V _{GS} =10V, I _D =2.0A (Note 1, 2)		19		nC
Gate to Source Charge		Q _{GS}			8		nC
Gate to Drain Charge		Q _{GD}			4		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =2.0A, R _G =25Ω (Note 1, 2)		14		ns
Rise Time		t _R			20		ns
Turn-OFF Delay Time		t _{D(OFF)}			36		ns
Fall-Time		t _F			47		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				2	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				6	A
Diode Forward Voltage		V _{SD}	I _F =2.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =2.0A, V _{GS} =0V,		868		ns
Reverse Recovery Charge (Note 1)		Q _{rr}	dl _F /dt = 100 A/μs		3.9		uC

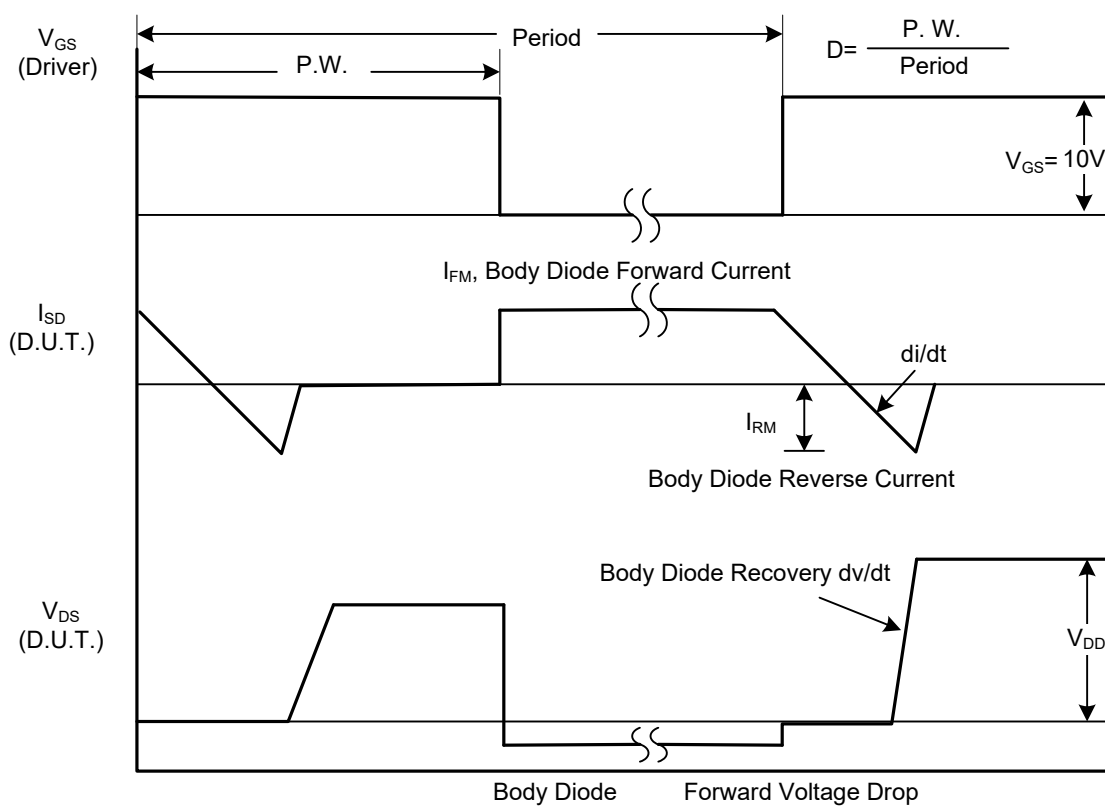
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

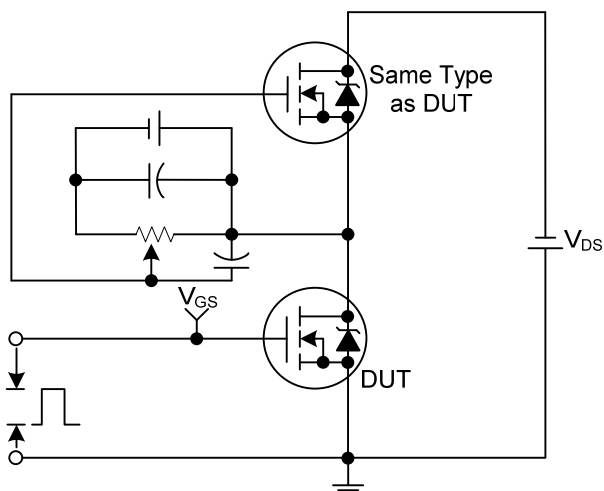


Peak Diode Recovery dv/dt Test Circuit

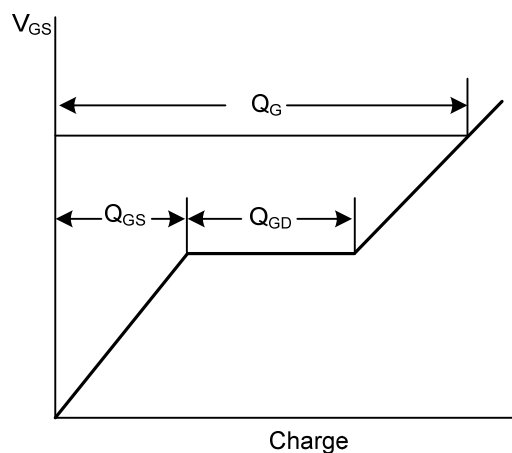


Peak Diode Recovery dv/dt Waveforms

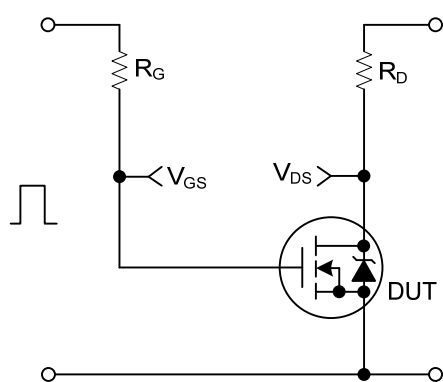
■ TEST CIRCUITS AND WAVEFORMS



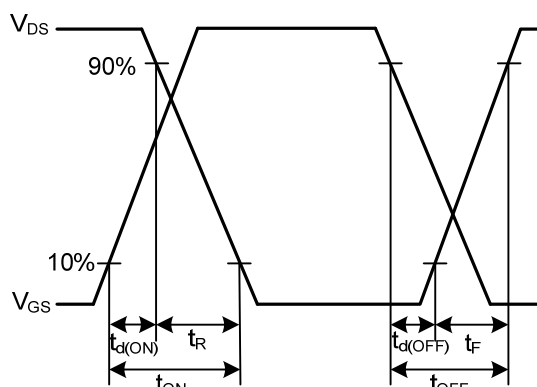
Gate Charge Test Circuit



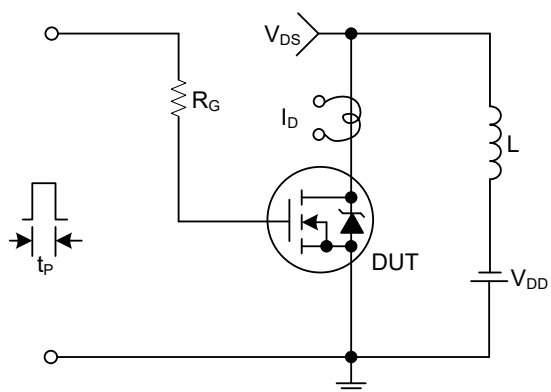
Gate Charge Waveforms



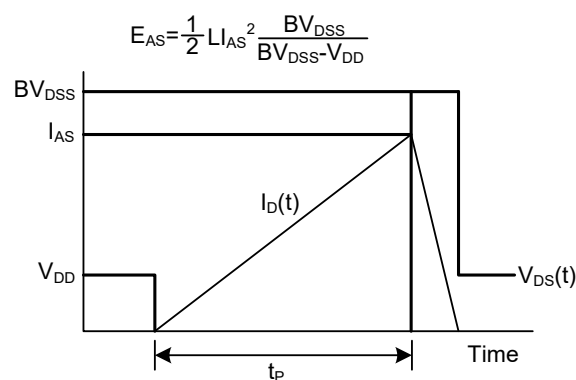
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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