



U74HC164A

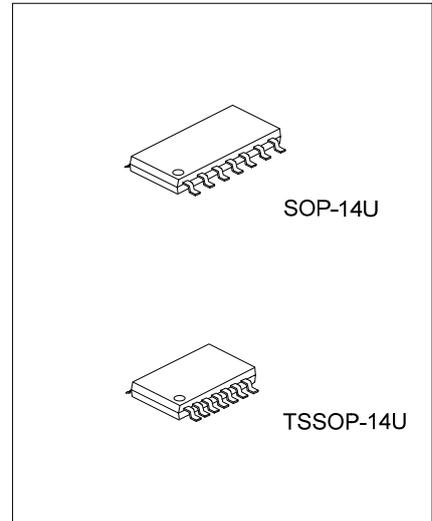
CMOS IC

8-BIT SERIAL-IN AND PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The **U74HC164A** is an 8-bit serial-in/parallel-out shift register.

The logical AND of the DSA and DSB enters into Q0 and shifts one place to right on each LOW-to-HIGH transition of the clock (\overline{CP}). A low level on the master reset (\overline{MR}) input clears all the registers asynchronously and force all outputs LOW.



FEATURES

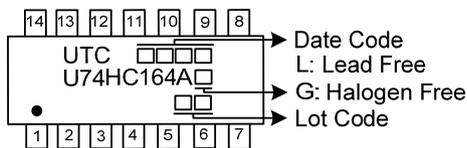
- * Operation Voltage Range: 2V ~ 6V
- * Asynchronous Reset Input

ORDERING INFORMATION

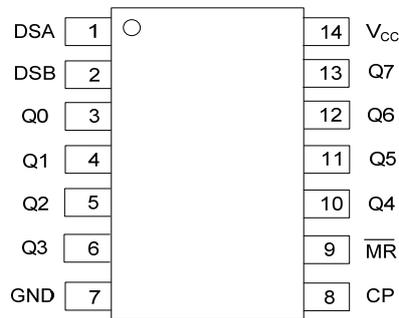
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC164AL-UEA-R	U74HC164AG-UEA-R	SOP-14U	Tape Reel
U74HC164AL-UEB-R	U74HC164AG-UEB-R	TSSOP-14U	Tape Reel

<p>U74HC164AG-UEA-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) UEA: SOP-14U, UEB: TSSOP-14U (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION



■ FUNCTION TABLE

OPERATING MODES	INPUT				OUTPUT	
	MR	CP	DSA	DSB	Q ₀	Q ₁ – Q ₇
Reset (clear)	L	X	X	X	L	L - L
Shift	H	↑	l	l	L	q ₀ – q ₆
	H	↑	l	h	L	q ₀ – q ₆
	H	↑	h	l	L	q ₀ – q ₆
	H	↑	h	h	H	q ₀ – q ₆

Notes: H = High voltage level.

L = Low voltage level.

h = High voltage level one set-up time prior to the low-to-high clock transition.

l = Low voltage level one set-up time prior to the low-to-high clock transition.

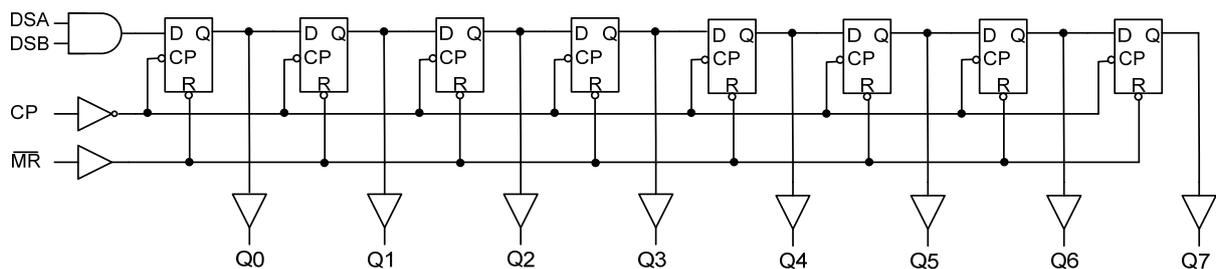
X = Don't care.

↑ = Transition from low to high level.

q_n = Lower case letters indicate the state of the referenced input one set-up time prior to the low-to-high clock transition.

■ FUNCTIONAL DIAGRAM

Logic Diagram



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7	V
V_{CC} or GND Current	I_{CC}		±50	mA
Output Current	I_{OUT}	$V_{OUT}=0$ to V_{CC}	±25	mA
Input Clamp Current (Note 2)	I_{IK}	$V_{IN}<0$ or $V_{IN}>V_{CC}$	±20	mA
Output Clamp Current (Note 2)	I_{OK}	$V_{OUT}<0$ or $V_{OUT}>V_{CC}$	±20	mA
Storage Temperature	T_{STG}		-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0		6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Time	t_R / t_F	$V_{CC}=2V$			1000	ns
		$V_{CC}=4.5V$			500	ns
		$V_{CC}=6V$			400	ns
Operating Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-14U	125	°C/W
	TSSOP-14U	150	°C/W

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage High-Level	V_{IH}	$V_{CC}=2.0V$	1.5			V
		$V_{CC}=4.5V$	3.15			V
		$V_{CC}=6.0V$	4.2			V
Input Voltage Low-Level	V_{IL}	$V_{CC}=2.0V$			0.5	V
		$V_{CC}=4.5V$			1.35	V
		$V_{CC}=6.0V$			1.8	V
Output Voltage High-Level	V_{OH}	$V_{CC}=2.0V, I_{OH}=-20\mu A$	1.9			V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4			V
		$V_{CC}=6.0V, I_{OH}=-20\mu A$	5.9			V
		$V_{CC}=4.5V, I_{OH}=-4mA$	3.98			V
		$V_{CC}=6.0V, I_{OH}=-5.2mA$	5.48			V
Output Voltage Low-Level	V_{OL}	$V_{CC}=2.0V, I_{OL}=20\mu A$			0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$			0.1	V
		$V_{CC}=6.0V, I_{OL}=20\mu A$			0.1	V
		$V_{CC}=4.5V, I_{OL}=4mA$			0.26	V
		$V_{CC}=6.0V, I_{OL}=5.2mA$			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=V_{CC}$ or GND, $V_{CC}=6.0V$			±0.1	μA
Quiescent Supply Current	I_Q	$V_{IN}=V_{CC}$ or GND, $V_{CC}=6.0V, I_{OUT}=0$			8	μA
Input Capacitance	C_{IN}				10	pF

■ DYNAMIC CHARACTERISTICS

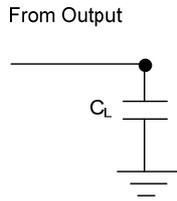
(GND=0V, $t_R=t_F=6ns$, $C_L=50pF$, $T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From CP to Qn	t_{PHL}, t_{PLH}	$V_{CC}=2.0V$		89	175	ns
		$V_{CC}=4.5V$		26	45	ns
		$V_{CC}=6.0V$		20	35	ns
Propagation Delay From \overline{MR} to Qn	t_{PHL}	$V_{CC}=2.0V$		75	205	ns
		$V_{CC}=4.5V$		25	45	ns
		$V_{CC}=6.0V$		19	35	ns
Output Transition Time	t_{THL}, t_{TLH}	$V_{CC}=2.0V$		45	75	ns
		$V_{CC}=4.5V$		20	35	ns
		$V_{CC}=6.0V$		14	25	ns
Clock Pulse Width High or Low	t_w	$V_{CC}=2.0V$	80			ns
		$V_{CC}=4.5V$	16			ns
		$V_{CC}=6.0V$	14			ns
Master Reset Pulse Width Low	t_w	$V_{CC}=2.0V$	100			ns
		$V_{CC}=4.5V$	20			ns
		$V_{CC}=6.0V$	17			ns
Removal Time \overline{MR} to CP	t_{rem}	$V_{CC}=2.0V$	100			ns
		$V_{CC}=4.5V$	20			ns
		$V_{CC}=6.0V$	17			ns
Setup Time DSA and DSB to CP	t_{su}	$V_{CC}=2.0V$	100			ns
		$V_{CC}=4.5V$	20			ns
		$V_{CC}=6.0V$	17			ns
Hold Time DSA and DSB to CP	t_h	$V_{CC}=2.0V$	5			ns
		$V_{CC}=4.5V$	5			ns
		$V_{CC}=6.0V$	5			ns
Maximum Clock Pulse Frequency	f_{MAX}	$V_{CC}=2.0V$	6			MHz
		$V_{CC}=4.5V$	31			MHz
		$V_{CC}=6.0V$	36			MHz
Clock Frequency	f_{CLOCK}	$V_{CC}=2.0V$			6	MHz
		$V_{CC}=4.5V$			31	MHz
		$V_{CC}=6.0V$			36	MHz

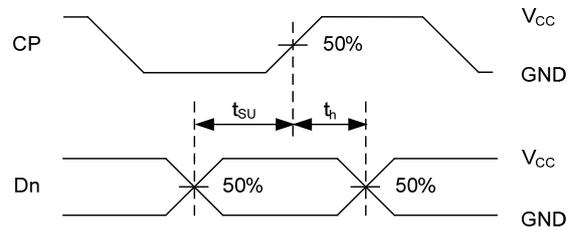
■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		40		pF

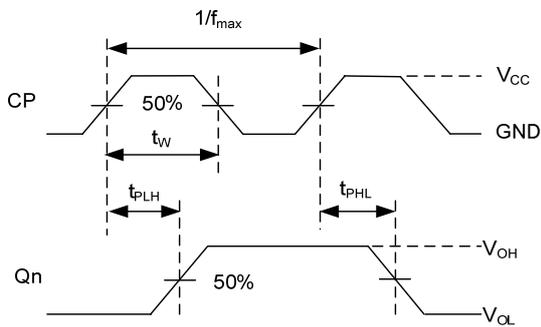
■ TEST CIRCUIT AND WAVEFORMS



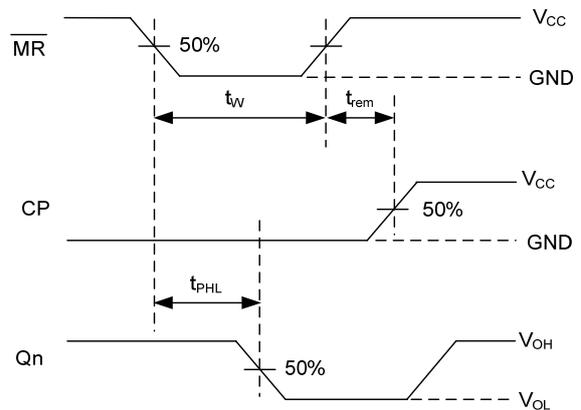
TEST CIRCUIT



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES FROM CP TO Qn



PROPAGATION DELAY TIMES FROM \overline{MR} TO Qn

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