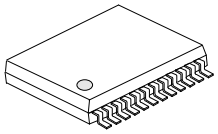
REMOTE 16-BIT I²C AND SMBUS I/O EXPANDER WITH INTERRUPT OUTPUT AND CONFIGURATION REGISTERS



TSSOP-24

■ DESCRIPTION

The UTC **UCA9555** is a low standby current I/O expansion with 24-pins,which can provide 16-bit general parallel input/output expansion for I²C bus. **UCA9555** has three hardware address bits, These three hardware address bits allow up to eight devices to share the same I²C-bus.

The UTC **UCA9555** has power-on reset function. When power-on and reaching a certain voltage, the internal state machine will be initialized and the register will be set to the default value. The open-break interrupt output of **UCA9555** will be activated when the input state is different from its corresponding input port register state and will send an indication to the system.

The UTC **UCA9555** has 16 I/O ports, which are divided into two groups, each group has 8 I/O ports. These two groups of I/O ports can be used as input ports or output ports. UTC **UCA9555** is used for push buttons, fans, LEDs, sensors, etc. when these devices require additional I/O, UTC **UCA9555** can provide a solution. In addition, it also has the function of polarity inversion, which can be selected through the register. The system master can enables the corresponding register by writing the corresponding byte to realize the corresponding function.

■ FEATURES

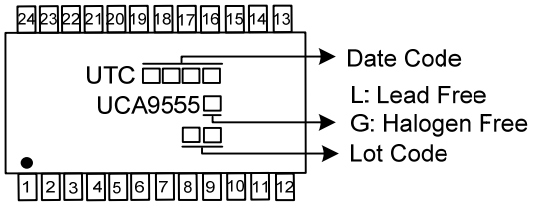
* Operating voltage is 2.3V to 5.5V
* The standby current is low
* SCL/SDA has an input filter
* Power-on reset
* 5 V tolerant I/Os
* The interrupt output is low
* Polarity Inversion register
* Address by Three Hardware Address Pins for Use of up to Eight Devices
* 16 I/O pins which default to 16 inputs
* 400kHz Fast-mode I²C-bus

■ ORDERING INFORMATION

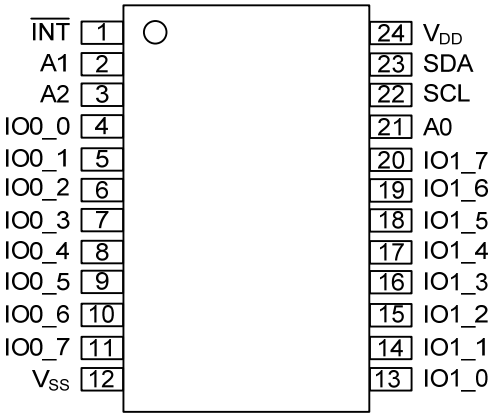
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCA9555G-P24-R	UCA9555G-P24-R	TSSOP-24	Tape Reel

UCA9555G-P24-R (1)Packing Type (2)Package Type (3)Green Package	 (1) R: Tape Reel (2) P24: TSSOP-24 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



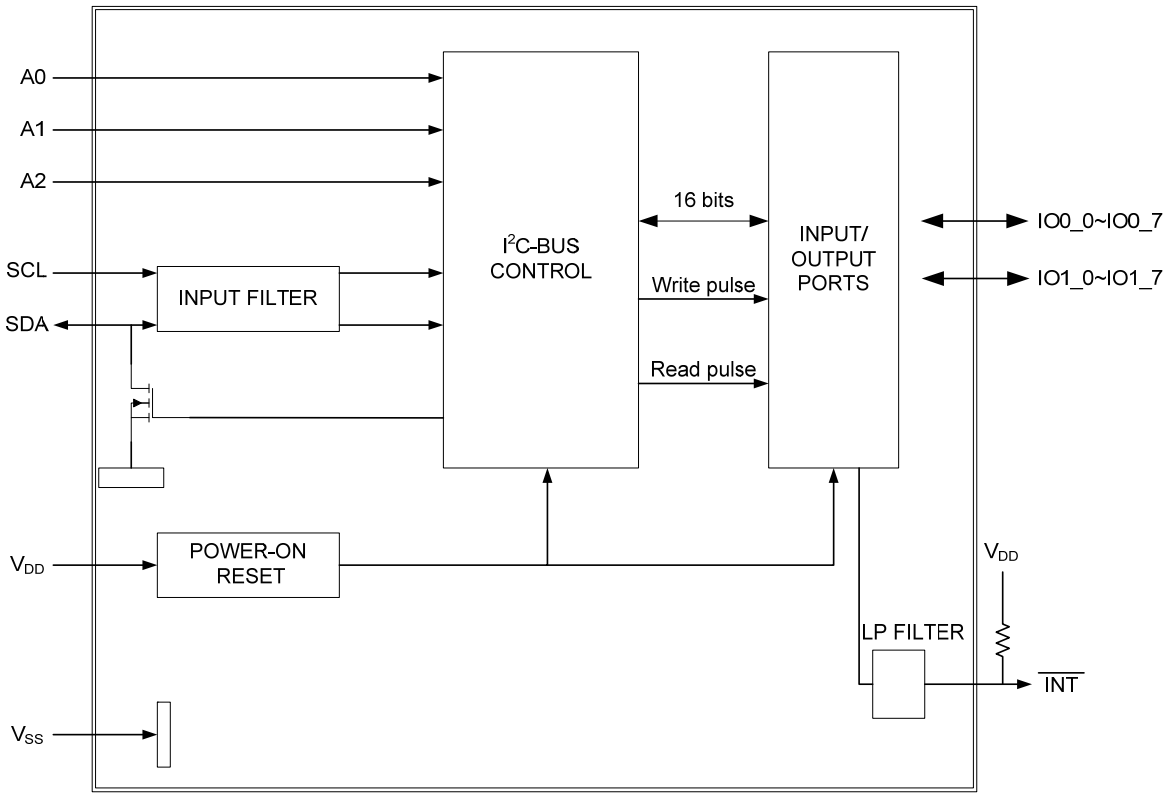
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{INT}$	Interrupt Output (Open-Drain)
2	A1	Address Input 1
3	A2	Address Input 2
4	IO0_0	Port 0 Input/Output
5	IO0_1	Port 0 Input/Output
6	IO0_2	Port 0 Input/Output
7	IO0_3	Port 0 Input/Output
8	IO0_4	Port 0 Input/Output
9	IO0_5	Port 0 Input/Output
10	IO0_6	Port 0 Input/Output
11	IO0_7	Port 0 Input/Output
12	V_{SS}	Supply Ground
13	IO1_0	Port 1 Input/Output
14	IO1_1	Port 1 Input/Output
15	IO1_2	Port 1 Input/Output
16	IO1_3	Port 1 Input/Output
17	IO1_4	Port 1 Input/Output
18	IO1_5	Port 1 Input/Output
19	IO1_6	Port 1 Input/Output
20	IO1_7	Port 1 Input/Output
21	A0	Address Input 0
22	SCL	Serial Clock Line
23	SDA	Serial Data Line
24	V_{DD}	Supply Voltage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage Range	V_{DD}		-0.5 ~ 6	V
Voltage On an Input/Output Pin	$V_{I/O}$		V_{SS}-0.5 ~ 6	V
Output Current	I_O	On an I/O Pin	±50	mA
Input Current	I_I		±20	mA
Supply Current	I_{DD}		160	mA
Ground Supply Current	I_{SS}		200	mA
Maximum Junction Temperature	$T_{J(MAX)}$		+125	°C
Storage Temperature	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	115	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		2.3		5.5	V
Operating Free-Air Temperature	T_{OPR}		-40		+85	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLIES						
Supply Current	I_{DD}	Operating Mode, V_{DD}=5.5V No Load, f_{SCL}=100kHz		100		μA
Standby Current	I_{STB}	Standby Mode, V_{DD}=5.5V No load, V_I=V_{SS}, f_{SCL}=0kHz, I/O=Inputs		0.8	1.5	μA
		Standby Mode, V_{DD}=5.5V No load, V_I=V_{SS}, f_{SCL}=0kHz, I/O=Inputs		0.25	1	μA
Power-On Reset Voltage	V_{POR}	No Load, V_I=V_{DD} or V_{SS}		1.7	2.2	V
INPUT SCL, INPUT/OUTPUT SDA						
LOW-Level Input Voltage	V_{IL}				0.3× V_{DD}	V
HIGH- Level Input Voltage	V_{IH}		0.7× V_{DD}			V
LOW-Level Output Current	I_{OL}	V_{OL}=0.4V	3			mA
Leakage Current	I_L	V_I=V_{DD}=V_{SS}	-1		1	μA
Input Capacitance (Input SCL)	C_I	V_I=V_{SS}		7		pF
Input Capacitance (Input SDA)	C_I	V_I=V_{SS}		7		pF
I/Os						
LOW-Level Input Voltage	V_{IL}				0.3× V_{DD}	V
HIGH- Level Input Voltage	V_{IH}		0.7× V_{DD}			V
LOW-Level Output Current	I_{OL}	V_{DD}=2.3V to 5.5V, V_{OL}=0.5V	8	12		mA
		V_{DD}=2.3V to 5.5V, V_{OL}=0.7V	10	16		mA

■ RECOMMENDED OPERATING CONDITIONS (Cont.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
I/Os						
HIGH-Level Output Current	V_{OH}	I_{OH}=-8mA, V_{DD}=2.3V	1.8			V
		I_{OH}=-10mA, V_{DD}=2.3V	1.7			V
		I_{OH}=-8mA, V_{DD}=3.0V	2.6			V
		I_{OH}=-10mA, V_{DD}=3.0V	2.5			V
		I_{OH}=-8mA, V_{DD}=4.75V	4.1			V
		I_{OH}=-10mA, V_{DD}=4.75V	4			V
HIGH-Level Input Leakage Current	I_{LIH}	V_{DD}=5.5V, V_I=V_{DD}			1	μA
LOW-Level Input Leakage Current	I_{LIL}	V_{DD}=5.5V, V_I=V_{SS}			-100	μA
input capacitance	C_I			4		pF
output capacitance	C_O			4		pF
INTERRUPT INT						
LOW-Level Output Current	I_{OL}	V_{OL}=0.4V	3			mA
SELECT INPUTS A0, A1, A2						
LOW-Level Input Voltage	V_{IL}				0.3× V_{DD}	V
HIGH- Level Input Voltage	V_{IH}		0.7× V_{DD}			V
Input Leakage Current	I_{LI}		-1		1	μA

Notes: 1. V_{DD} must be lowered to 0.2V for at least 10μs in order to reset part.
2. Each I/O must be externally limited to a maximum of 25mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100mA for a device total of 200mA.
3. The total current sourced by all I/Os must be limited to 160mA.

■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Standard-Mode			Fast-Mode			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SCL Clock Frequency	f_{SCL}		0		100	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		4.7			1.3			μs
Hold Time (Repeated) START Condition	$t_{HD;STA}$		4.0			0.6			μs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$		4.7			0.6			μs
Set-Up Time for STOP Condition	$t_{SU;STO}$		4.0			0.6			μs
Data Valid Acknowledge Time	$t_{VD;ACK}$				4.45			1.9	μs
Data Hold Time	$t_{HD;DAT}$		0			0			ns
Data Valid Time	$t_{VD;DAT}$				4.45			1.9	ns
Data Set-Up Time	$t_{SU;DAT}$		250			100			ns
LOW Period of The SCL Clock	t_{LOW}		4.7			1.3			μs
HIGH Period of The SCL Clock	t_{HIGH}		4.0			0.6			μs
Fall Time of Both SDA and SCL Signals	t_f				300	20+ 0.1C_b		300	ns
Rise Time of Both SDA and SCL Signals	t_r				1000	20+ 0.1C_b		300	ns
Pulse Width of Spikes That Must be Suppressed By The Input filter	t_{SP}				50			50	ns

■ DYNAMIC CHARACTERISTICS (Cont)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
PORT TIMING									
Data Output Valid Time	$t_{V(Q)}$				200			200	ns
Data Input Set-Up Time	$t_{SU(D)}$		150			150			ns
Data Input Hold Time	$t_{h(D)}$		1			1			μs
INTERRUPT TIMING									
Valid Time on Pin $\overline{INT}$	$t_{v(INT\_N)}$				4			4	μs
Reset Time on Pin $\overline{INT}$	$t_{rst(INT\_N)}$				4			4	μs

Notes: 1. $t_{VD,\ ACK}$ = Time for acknowledgement signal from SCL LOW to SDA (out) LOW.
2. $t_{VD,\ DAT}$ = Minimum time for SDA data out to be valid following SCL LOW.
3. Cb = Total capacitance of one bus line in pF.
4. $t_{V(INT\_N)}$ is measured from 50% I_O input to 0.3×V_{DD} on $\overline{INT}$.
5. $t_{rst(INT\_N)}$ is measured from 0.3×V_{DD} on SCL to 0.7×V_{DD} on $\overline{INT}$.

■ PARAMETER MEASUREMENT INFORMATION

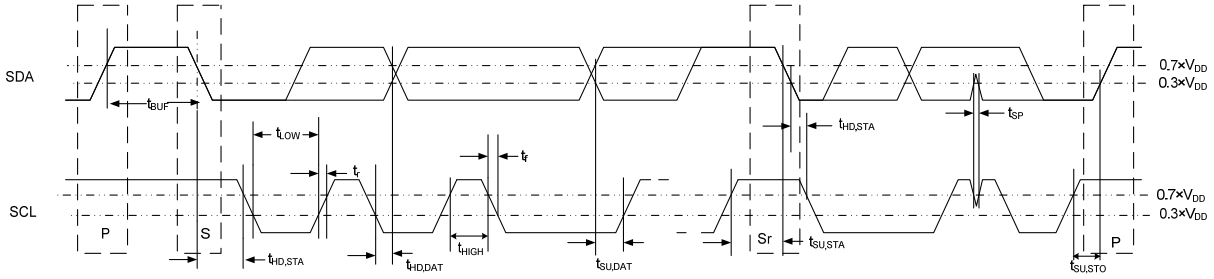
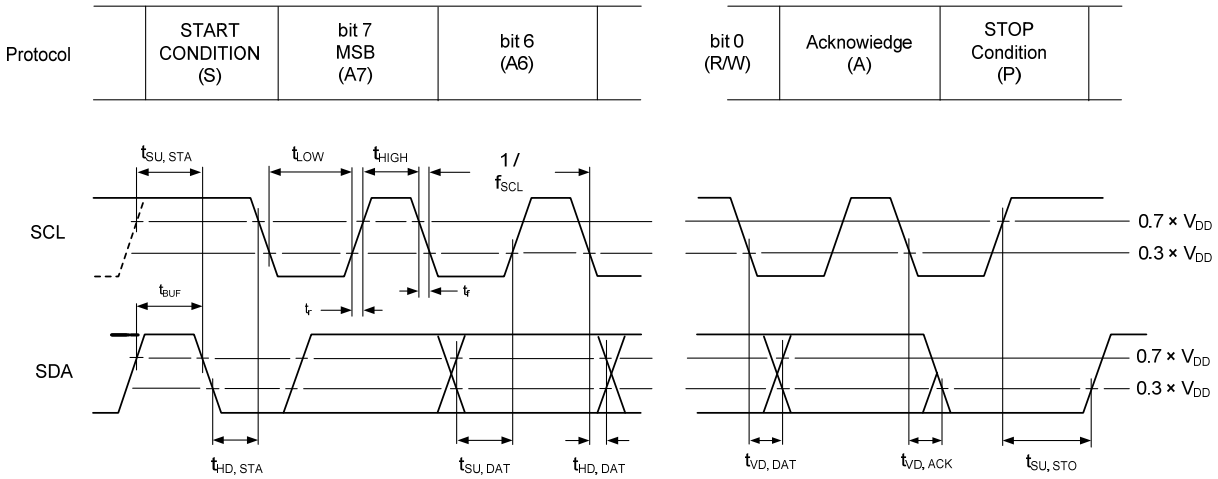


Figure 1. Definition of timing on the I²C-bus



Rise and fall times refer to V_{IL} and V_{IH}.

Figure 2. I²C-bus timing diagram

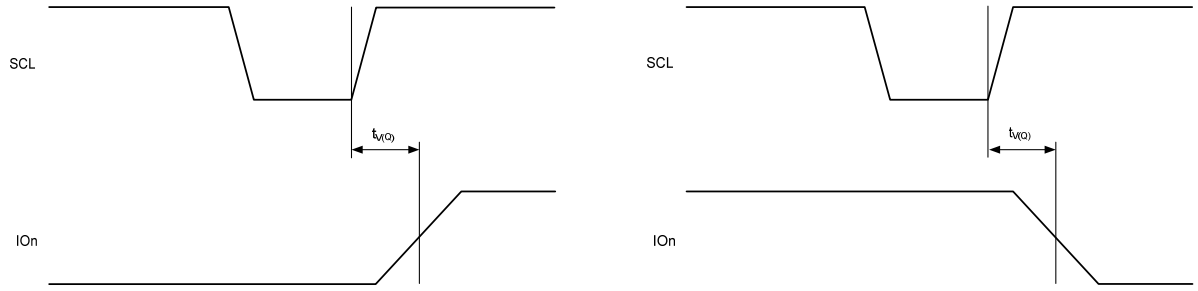


Figure 3. $t_{v(Q)}$ timing

■ REGISTER DESCRIPTION

The registers of **UCA9555** include input register, output register, polarity reversal register, and configuration register.

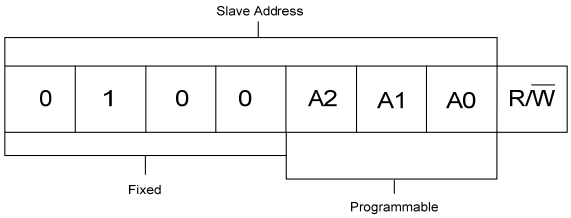


Figure 4. UCA9555 Device Address

Command byte

The command byte is entered after the address byte and is used as a pointer to determine which register to use.

B7	B6	B5	B4	B3	B2	B1	B0

Figure 5. Pointer register bits

Table 1. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	Read byte	xxxx xxxx
0	0	0	0	0	0	0	1	01h	Input port 1	Read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02h	Output port 0	Read/Write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	Read/Write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity inversion port 0	Read/Write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity inversion port 1	Read/Write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	Read/Write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	Read/Write byte	1111 1111

Note: The default value 'X' is determined by the externally applied logic level.

Registers 0 and 1: Input port registers

The input port register is used to represent the input logic of the pin. It is only active during the read operation and has no effect on whether the pin is defined as input or output by the configuration register. The default value X is determined by the logical level of the pin.

In addition, it is important to know that before the read operation, a write operation is required to give the I^2C device an indication that the input port register is to be used next.

Table 2. Input Port 0 Register

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symol	IO0_7	IO0_6	IO0_5	IO0_4	IO0_3	IO0_2	IO0_1	IO0_0
Default	X	X	X	X	X	X	X	X

Table 3. Input Port 1 Register

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symol	IO1_7	IO1_6	IO1_5	IO1_4	IO1_3	IO1_2	IO1_1	IO1_0
Default	X	X	X	X	X	X	X	X

■ REGISTER DESCRIPTION (Cont.)

Registers 2 and 3: Output port registers

When the configuration register is defined as output, the output port register displays the logic level of the pin. When the configuration register is defined as input, the value of the output port register has no effect on the logic level of the pin. Thus, the value read from this register reflects the value in the trigger that controls the output selection, not the logic level of the actual pin.

Table 4. Output Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symol	IO0_7	IO0_6	IO0_5	IO0_4	IO0_3	IO0_2	IO0_1	IO0_0
Default	1	1	1	1	1	1	1	1

Table 5. Output Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symol	IO1_7	IO1_6	IO1_5	IO1_4	IO1_3	IO1_2	IO1_1	IO1_0
Default	1	1	1	1	1	1	1	1

Registers 4 and 5: Polarity inversion registers

This register allows the user to invert the polarity of the input port register. If this register is written with a 1, the input port data polarity is reversed, and if the input port data polarity is preserved, it can be cleared by writing a 0 to the register.

Table 6. Polarity inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symol	IO0_7	IO0_6	IO0_5	IO0_4	IO0_3	IO0_2	IO0_1	IO0_0
Default	0	0	0	0	0	0	0	0

Table 7. Polarity inversion port 1 register

Bit	7	6	5	4	3	2	1	0
Symol	IO1_7	IO1_6	IO1_5	IO1_4	IO1_3	IO1_2	IO1_1	IO1_0
Default	0	0	0	0	0	0	0	0

Registers 6 and 7: Configuration registers

The input port register is used to represent the input logic of the pin. It is only active during the read operation and has no effect on whether the pin is defined as input or output by the configuration register. The default value X is determined by the logical level of the pin.

In addition, it is important to know that before the read operation, a write operation is required to give the I^2C device an indication that the input port register is to be used next.

Table 8. Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symol	IO0_7	IO0_6	IO0_5	IO0_4	IO0_3	IO0_2	IO0_1	IO0_0
Default	1	1	1	1	1	1	1	1

Table 9. Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symol	IO1_7	IO1_6	IO1_5	IO1_4	IO1_3	IO1_2	IO1_1	IO1_0
Default	1	1	1	1	1	1	1	1

■ REGISTER DESCRIPTION (Cont.)

Power-on reset

As the supply voltage gradually increases from 0V, an internal power-on reset circuit keeps the **UCA9555** in the reset state until the supply voltage reaches V_{POR}, at which point the reset condition is released and the **UCA9555** register and the internal circuit state machine are initialized to their default state. After that, the V_{DD} must be reduced to below 0.2V and restored to the operating voltage for the power-on reset to be performed again.

I/O PORT

When the I/O port is configured as input, FETs Q1 and Q2 are off, creating a high-impedance input that is weakly pulled up to V_{DD}. The input voltage can be increased to a maximum of 5.5V above V_{DD}.

When the I/O port is configured as an output, either FETs Q1 or Q2 is turned on, depending on the state of the output port register. Due to the low impedance path between the pin and the V_{DD} or V_{SS}, special care needs to be taken if an external voltage is applied to I/O configured as an output.

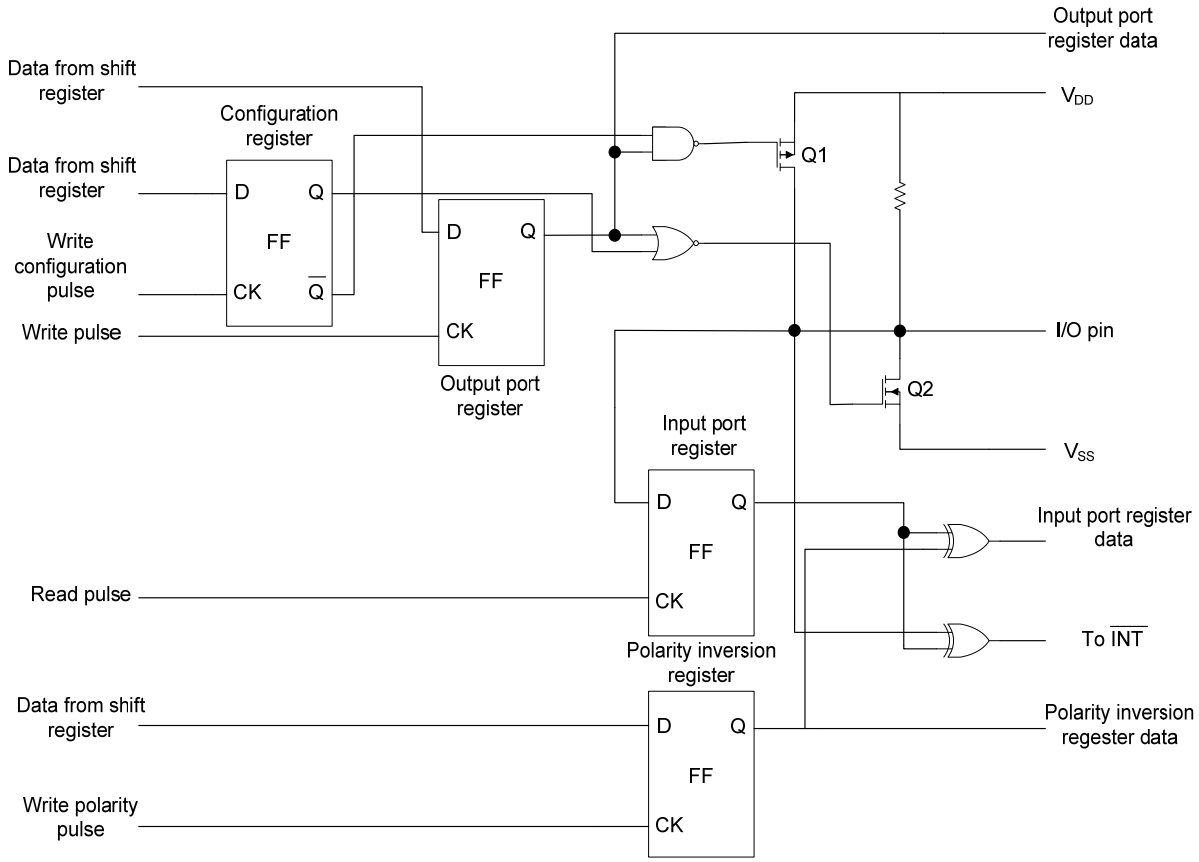


Figure 6. Simplified schematic of I/Os

■ REGISTER DESCRIPTION (Cont.)

Bus transactions

Writing to the port registers

Data is transferred to the **UCA9555** by sending the device address and setting the minimum logical bit to 0. After this, the command byte is sent and it is determined which register will receive the data after the command byte.

The eight registers in the **UCA9555** are configured to operate with four register pairs, which are the input port register, output port register, polarity reversal port register, and configuration port register. After sending data to one register, the next data byte will be sent to another register in the pair.

There is no limit to the number of bytes of data sent in a single write, so that each eight-bit register can be updated independently of the others.

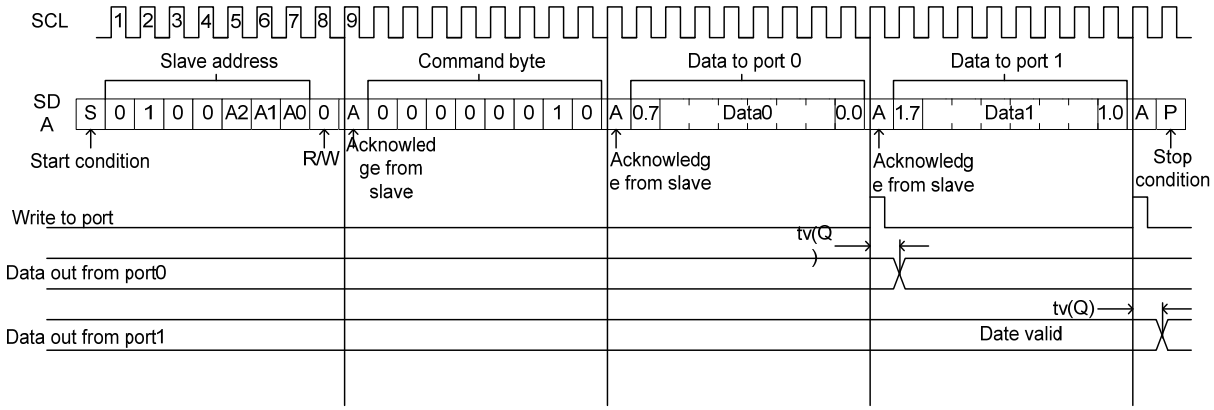


Figure 7. Write to output port registers

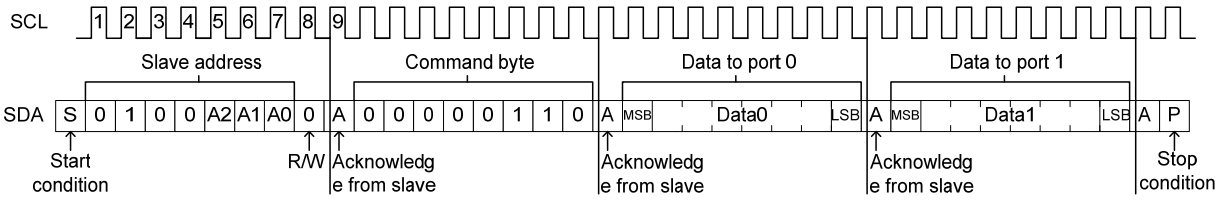


Figure 8. Write to configuration registers

■ REGISTER DESCRIPTION (Cont.)

Reading the port registers

In order to read data from the **UCA9555**, the bus master must first set the lowest logical value of the address byte to 0, and then send a command byte to determine which register to access. It then restarts and sends the device address again, but this time the lowest logical address byte is set to 1, after which the data in the register defined by the command byte is sent by the **UCA9555**.

When data is read by one register in the pair, another byte will be read by the other register. For example, if you read input port 1, the next byte read will be input port 0. There is no limit to the number of data bytes received in a read transfer, but the bus host cannot acknowledge the data after the final byte is received.

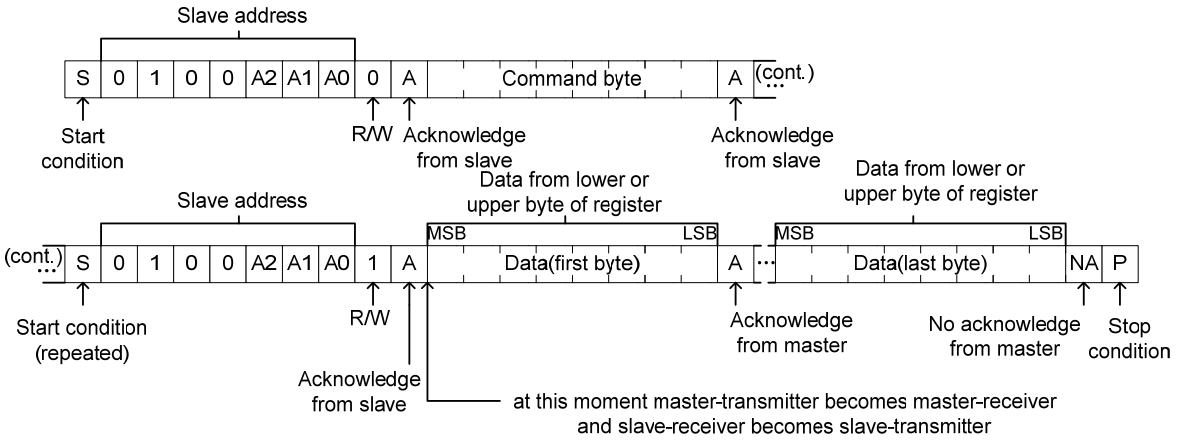
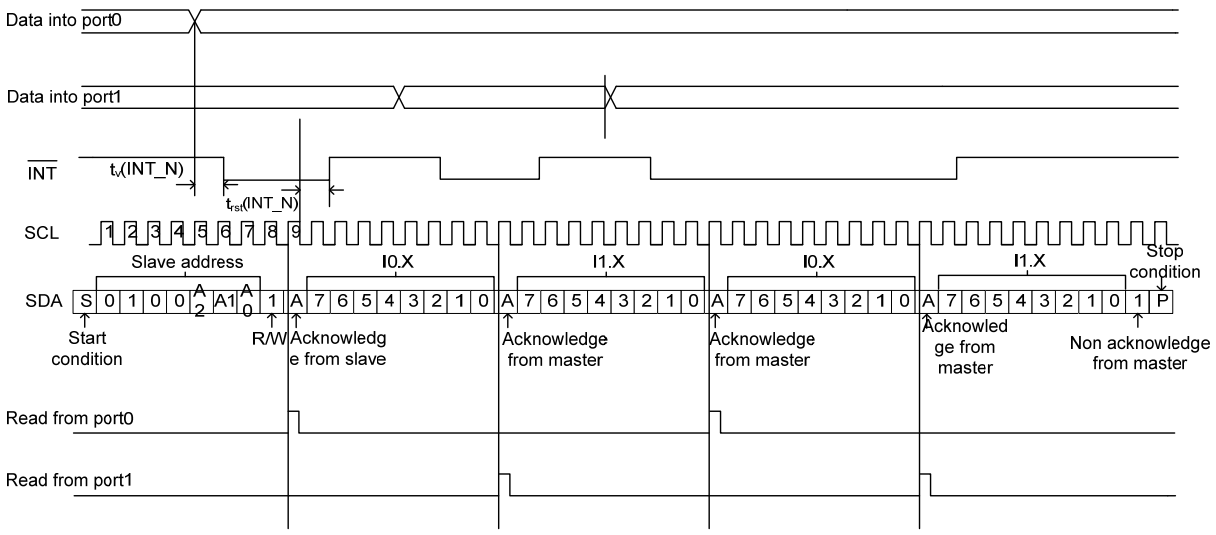


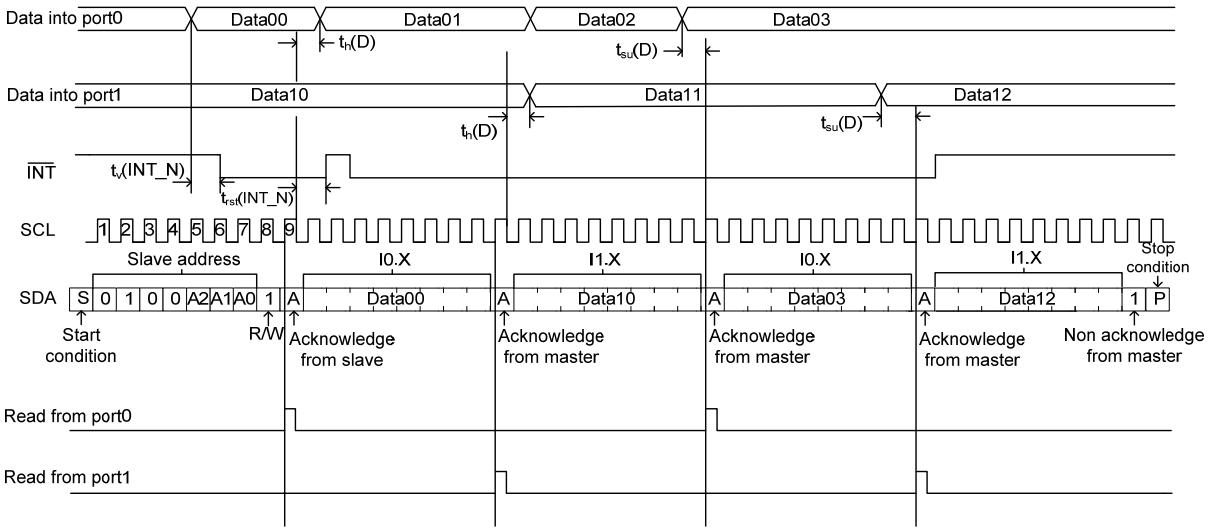
Figure 9. Read from register



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It
is assumed that the command byte has previously been set to '00' (read Input Port register).

Figure 10. Read input port registers, scenario 1

■ REGISTER DESCRIPTION (Cont.)



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It
is assumed that the command byte has previously been set to '00' (read Input Port register).

Figure 11. Read input port registers, scenario 2

Interrupt output

The leak interrupt output is activated when the pins are configured as inputs and one of the pins changes state. Interrupts are disabled when the input returns to its previous state or when the input register is read. No interrupt is caused when the pin is configured as an output.

Remark:

1. Each 8-bit port is read independently, so an interrupt caused by port 0 will not be cleared by a read or vice versa on port 1, and an interrupt caused by a read or vice versa on port 0.
2. Changing the pin from output to input may result in an error interrupt when the state of the pin does not match the contents of the input port register.

■ CHARACTERISTICS OF THE I²C-BUS

The I²C bus is a bidirectional, dual-wire synchronous serial bus that requires only SDA and SCL to transmit information between devices connected to the bus.

When connected to the output stage of the device, the two wires must be connected to the power supply via a pull-up resistor, and data transfer can only be started when the bus is not busy.

Bit transfer

When transmitting data, the data on the SDA must remain stable during clock high levels, and data changes are only allowed during clock low levels, so changes in the SDA data lines can account for bit control signals during clock high levels.

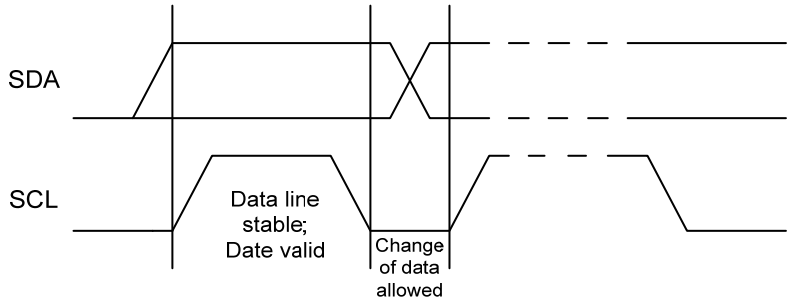


Figure 12. Bit transfer

■ CHARACTERISTICS OF THE I²C-BUS (Cont.)

Start and stop conditions

Both the data and clock lines remain high when the bus is not busy. When the clock is on high power level, the change from high to low data on the data line is defined as the starting condition; The change in data from low to high on the data line is defined as the stop condition.

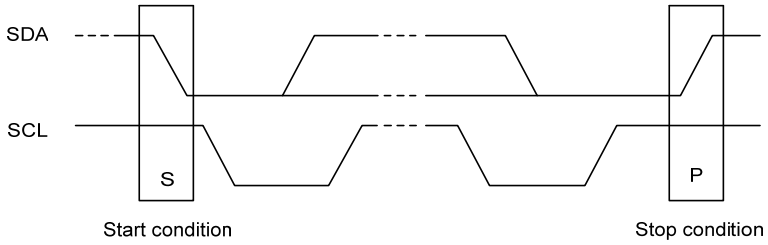


Figure 13. Definition of start and stop conditions

System configuration

A device generating a message is the ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

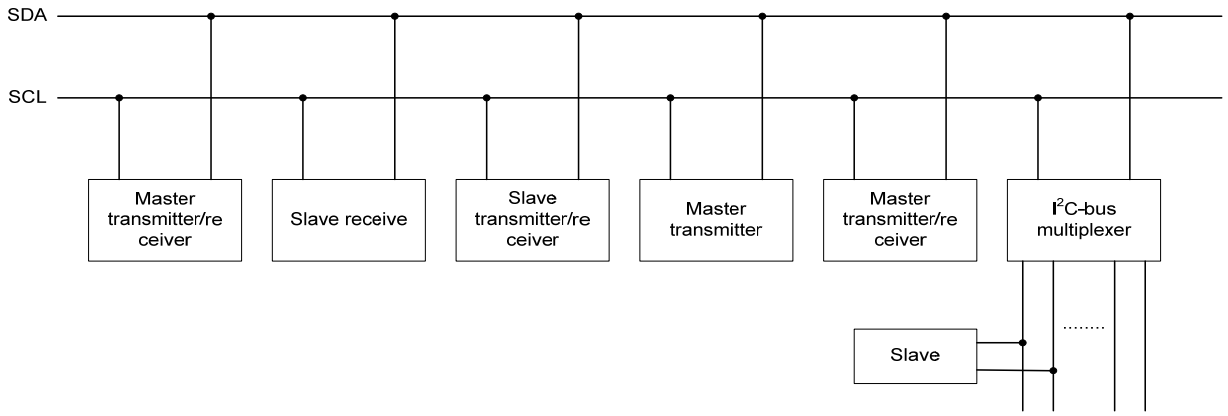


Figure 14. System configuration

Acknowledge

Any number of data words is sent directly from the transmitter to the receiver between the start and the stop conditions. Each 8-bit byte is followed by an ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. Setup and hold times must be met to ensure proper operation.

The master receiver no longer generates an acknowledgement bit (NACK) after the last byte is sent from the output and signals the end of data to the slave transmitter. This is achieved by the transmitter by pulling the SDA line from low to high during the high level of the clock pulse.

■ CHARACTERISTICS OF THE I²C-BUS (Cont.)

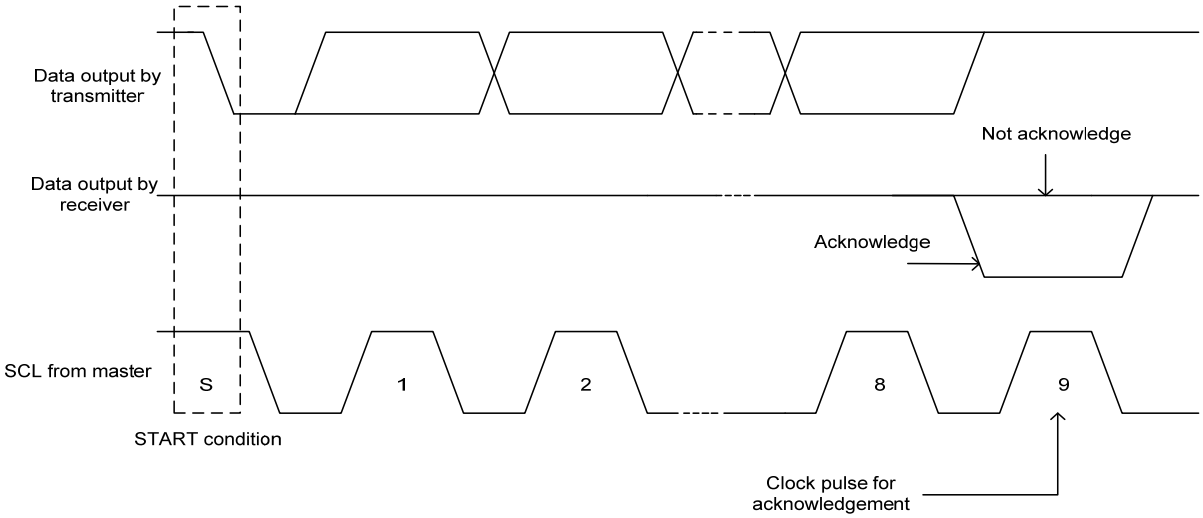
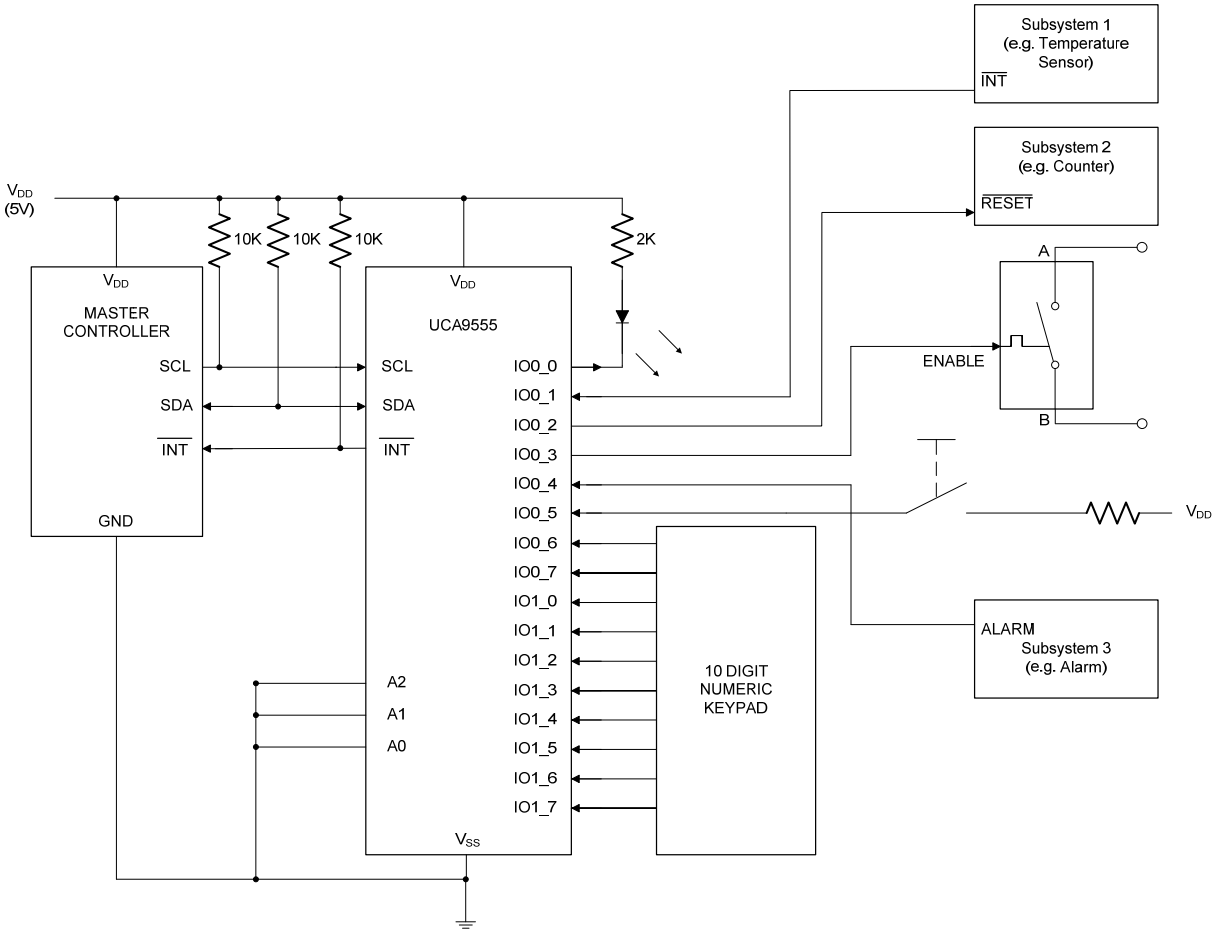


Figure 15. Acknowledgement on the I²C-bus

■ TYPICAL APPLICATION CIRCUIT



Device address configured as 0100000X for this example.
IO0_0, IO0_2, IO0_3 configured as outputs.
IO0_1, IO0_4 to IO0_7, and IO1_0 to IO1_7 configured as inputs.