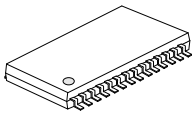
3-PHASE BRIDGE DRIVER



SOP-28

■ DESCRIPTION

The UTC **UTR2136** is high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600V.

■ FEATURES

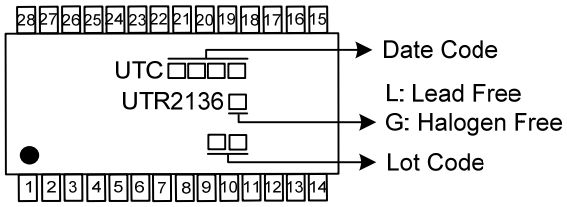
* Floating channel designed for bootstrap operation
* Fully operational to +600V
* Tolerant to negative transient voltage, dV/dt immune
* Gate drive supply range from 10V to 20V
* Undervoltage lockout for all channels
* Over-current shutdown turns off all six drivers
* Independent 3 half-bridge drivers
* Matched propagation delay for all channels
* Cross-conduction prevention logic
* Low side output out of phase with inputs. High side outputs out of phase
* 3.3 V logic compatible
* Lower di/dt gate drive for better noise immunity
* Externally programmable delay for automatic fault clear

■ ORDERING INFORMATION

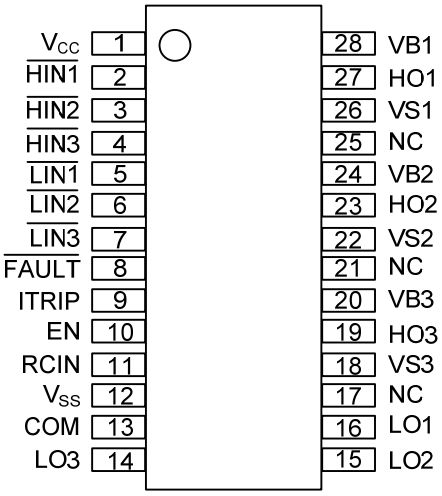
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UTR2136L-S28-R	UTR2136G-S28-R	SOP-28	Tape Reel

UTR2136G-S28-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S28: SOP-28 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



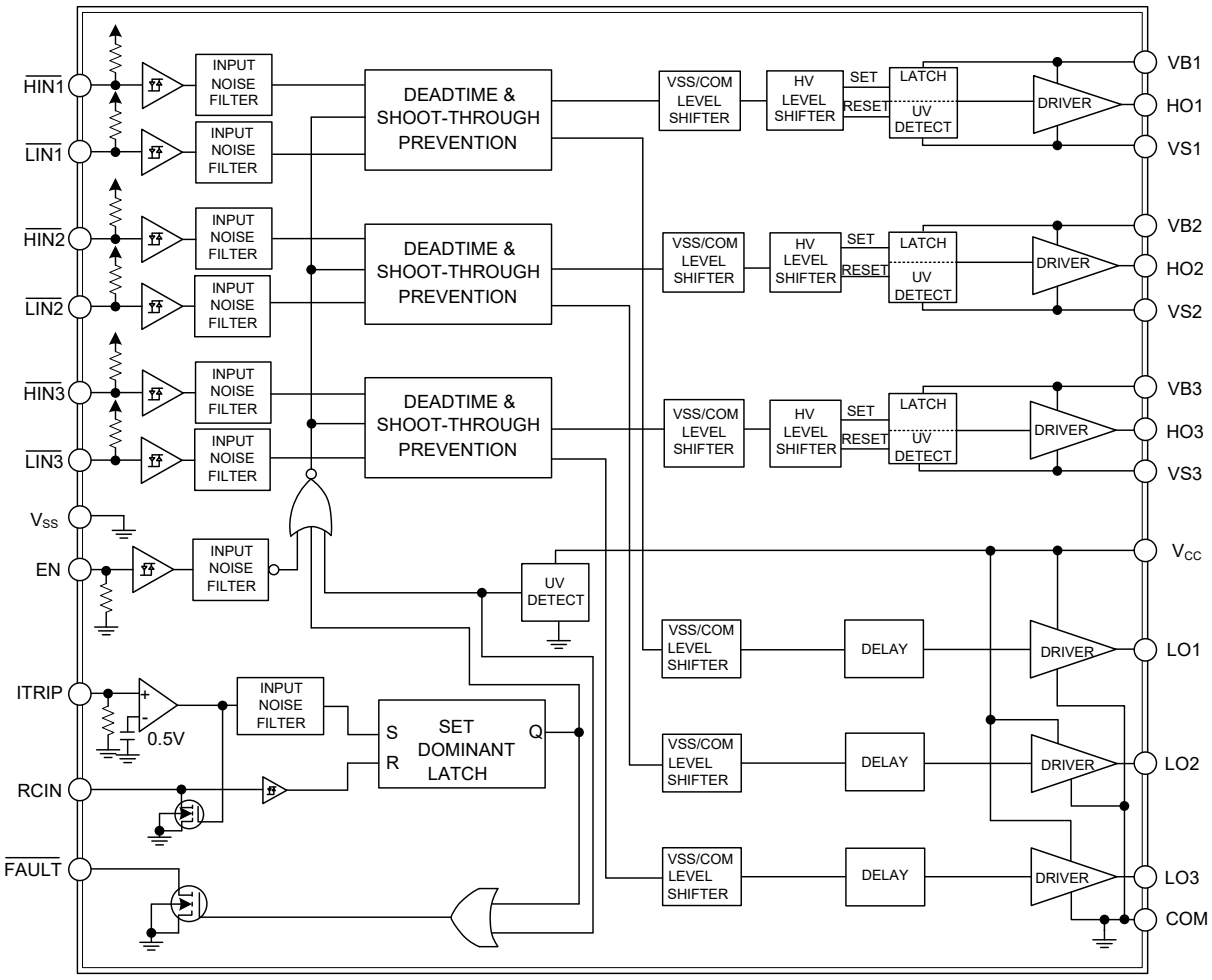
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN No.	PIN NAME	Description
1	V_{CC}	Low side and logic fixed supply
2, 3, 4	$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
5, 6, 7	$\overline{LIN1,2,3}$	Logic input for low side gate driver outputs (LO1,2,3), out of phase
8	$\overline{FAULT}$	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, opendrain output
9	ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time TFLTCLR, then automatically becomes inactive (open-drain high impedance).
10	EN	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high (i.e., positive logic) No effect on FAULT and not latched
11	RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
12	V_{SS}	Logic ground
13	COM	Low side gate drivers return
14	LO3	Low side gate driver outputs
15	LO2	Low side gate driver outputs
16	LO1	Low side gate driver outputs
17, 21, 25	NC	No connection
18	VS3	High voltage floating supply return
19	HO3	High side gate driver outputs
20	VB3	High side floating supply
22	VS2	High voltage floating supply return
23	HO2	High side gate driver outputs
24	VB2	High side floating supply
26	VS1	High voltage floating supply return
27	HO1	High side gate driver outputs
28	VB1	High side floating supply

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
High Side Offset Voltage	V_S	$V_{B\ 1,2,3}$ - 25 ~ $V_{B\ 1,2,3}$ + 0.3	V
High Side Floating Supply Voltage	V_B	-0.3 ~ 625	V
High Side Floating Output Voltage	V_{HO}	$V_{S1,2,3}$ - 0.3 ~ $V_{B\ 1,2,3}$ + 0.3	V
Low Side and Logic Fixed Supply Voltage	V_{CC}	-0.3 ~ 25	V
Logic Ground	V_{SS}	V_{CC} - 25 ~ V_{CC} + 0.3	V
Low Side Output Voltage	$V_{LO1,2,3}$	-0.3 ~ V_{CC} + 0.3	V
Input Voltage LIN, HIN, ITRIP, EN	V_{IN}	V_{SS} -0.3 ~ Lower of (V_{SS} + 15) or V_{CC} + 0.3)	V
RCIN Input Voltage	V_{RCIN}	V_{SS} -0.3 ~ V_{CC} + 0.3	V
$\overline{FAULT}$ Output Voltage	V_{FLT}	V_{SS} -0.3 ~ V_{CC} + 0.3	V
Allowable Offset Voltage Slew Rate	dV/dt	50	V/ns
Package Power Dissipation @ $T_A \le +25°C$	P_D	1.6	W
Thermal Resistance, Junction to Ambient	θ_{JA}	78	°C/W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55 ~ 150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High Side Floating Supply Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$ +10		$V_{S1,2,3}$ + 20	V
High Side Floating Supply Offset Voltage	$V_{S\ 1,2,3}$	(Note)		600	V
High Side Output Voltage	$V_{HO\ 1,2,3}$	$V_{S1,2,3}$		$V_{B1,2,3}$	V
Low Side Output Voltage	$V_{LO1,2,3}$	0		V_{CC}	V
Low Side and Logic Fixed Supply Voltage	V_{CC}	10		20	V
Logic Ground	V_{SS}	-5		5	V
$\overline{FAULT}$ Output Voltage	V_{FLT}	V_{SS}		V_{CC}	V
RCIN Input Voltage	V_{RCIN}	V_{SS}		V_{CC}	V
ITRIP Input Voltage	V_{ITRIP}	V_{SS}		V_{SS}+5	V
Logic input voltage $\overline{LIN}$, $\overline{HIN}$	V_{IN}	V_{SS}		V_{SS}+5	V
Ambient Temperature	T_A	-40		125	°C

Note: Logic operational for V_S of (COM - 5V) to (COM + 600V). Logic state held for V_S of (COM - 5V) to (COM -V_{BS}).

■ STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V unless otherwise specified. The V_{IN}, V_{TH}, and IIN parameters are referenced to V_{SS} and are applicable to all six channels ($\overline{HIN1,2,3}$ and $\overline{LIN1,2,3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1, 2,3 and LO1,2,3.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic “0” Input Voltage $\overline{LIN1,2,3}$ $\overline{HIN1,2,3}$	V_{IH}		3.0			V
Logic “1” Input Voltage $\overline{LIN1,2,3}$ $\overline{HIN1,2,3}$	V_{IL}				0.8	V
Enable Positive Going Threshold	$V_{EN,TH+}$				3	V
Enable Negative Going Threshold	$V_{EN,TH-}$		0.8			V
ITRIP Positive Going Threshold	$V_{IT,TH+}$		0.37	0.46	0.55	V
ITRIP Input Hysteresis	$V_{IT,HYS}$			0.07		V
RCIN Positive Going Threshold	$V_{RCIN,TH+}$			8		V
RCIN Input Hysteresis	$V_{RCIN,HYS}$			3		V
High Level Output Voltage, V_{BIAS} - V_O	V_{OH}	I_O = 20mA		0.9	1.4	V
Low Level Output Voltage, V_O	V_{OL}	I_O = 20mA		0.4	0.6	V
V_{CC} and V_{BS} Supply Undervoltage Positive Going Threshold	V_{CCUV+} V_{BSUV+}		8.0	8.7	9.8	V
V_{CC} and V_{BS} Supply Undervoltage Negative Going Threshold	V_{CCUV-} V_{BSUV-}		7.4	8.0	9.0	V
V_{CC} and V_{BS} Supply Undervoltage Lockout Hysteresis	V_{CCUVH} V_{BSUVH}		0.3	0.7		V
Offset Supply Leakage Current	I_{LK}	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 600V			50	μA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{IN} = 0V or 5V		40	120	μA
Quiescent V_{CC} Supply Current	I_{QCC}	V_{IN} = 0V or 5V		1.2	2.3	mA
Input Clamp Voltage (HIN, LIN, ITRIP and EN)	$V_{IN,CLAMP}$	I_{IN} =100μA	4.9	5.3	5.7	V
Input Bias Current (LOUT = HI)	I_{LIN+}	V_{LIN} = 5V		150	300	μA
Input Bias Current (LOUT = LO)	I_{LIN-}	V_{LIN} = 0V		100	220	μA
Input Bias Current (HOUT = HI)	I_{HIN+}	V_{HIN} = 5V		150	300	μA
Input Bias Current (HOUT = LO)	I_{HIN-}	V_{HIN} = 0V		100	220	μA
“High” ITRIP Input Bias Current	I_{ITRIP+}	V_{ITRIP} = 5V		30	100	μA
“Low” ITRIP Input Bias Current	I_{ITRIP-}	V_{ITRIP} = 0V		0	1	μA
“High” ENABLE Input Bias Current	I_{EN+}	V_{ENABLE} = 5V		30	100	μA
“Low” ENABLE Input Bias Current	I_{EN-}	V_{ENABLE} =0V		0	1	μA
RCIN Input Bias Current	I_{RCIN}	Vrcin= 0V or 15V		0	1	μA
Output High Short Circuit Pulsed Current	I_{O+}	V_O =0V, PW ≤10μs	120	200		mA
Output Low Short Circuit Pulsed Current	I_{O-}	V_O =15V, PW ≤10μs	250	350		mA
RCIN Low On Resistance	R_{on_RCIN}			50	100	Ω
$\overline{FAULT}$ Low On Resistance	R_{on_FAULT}			50	100	Ω

■ DYNAMIC ELECTRICAL CHARACTERISTICS

V_{CC} = V_{BS} = V_{BIAS} = 15V, $V_{S1,2,3}$ = V_{SS} = COM, T_A = 25°C and C_L = 1000pF unless otherwise specified..

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turn-On Propagation Delay	t_{ON}	V_{IN} = 0V & 5V	400	550	700	ns
Turn-Off Propagation Delay	t_{OFF}	V_{IN} = 0V & 5V	250	400	550	ns
Turn-On Rise Time	t_r	V_{IN} = 0V & 5V		125	190	ns
Turn-Off Fall Time	t_f	V_{IN} = 0V & 5V		50	75	ns
ENABLE Low to Output Shutdown Propagation Delay	t_{EN}	V_{IN}, V_{EN} = 0V or 5V	300	450	600	ns
ITRIP to Output Shutdown Propagation Delay	t_{ITRIP}	V_{ITRIP} = 5V	500	750	1000	ns
ITRIP Blanking Time	t_{bl}	V_{IN} = 0V or 5V, V_{ITRIP} = 5V	100	150		ns
ITRIP to $\overline{FAULT}$ Propagation Delay	t_{FLT}	V_{IN} = 0V or 5V, V_{ITRIP} = 5V	400	600	800	ns
Input Filter Time (HIN, LIN)	t_{FILIN}	V_{IN} = 0V & 5V	100	200		ns
FAULT Clear Time RCIN: R = 2MΩ, C = 1nF	t_{FLTCLR}	V_{IN} = 0V or 5V, V_{ITRIP} = 0V	1.3	1.65	2	ms
Deadtime	DT	V_{IN} = 0V & 5V	220	290	360	ns
Matching Delay ON and OFF	MT	External dead time >400ns		40	75	ns
Matching Delay, max (t_{on}, t_{off}) - min (t_{on}, t_{off}), (t_{on}, t_{off} are applicable to all 3 channels)	MDT	External dead time >400ns		25	70	ns
Output Pulse Width Matching (pwin-pwout)	PM			40	75	ns

V_{CC}	**VBS**	**ITRIP**	**ENABLE**	**FAULT**	**LO1, 2, 3**	**HO1, 2, 3**
< UVCC	X	X	X	0 (Note 1)	0	0
15V	<UVBS	0V	5V	high imp	LIN1, 2, 3	0
15V	15V	0V	5V	high imp	LIN1, 2, 3	HIN1, 2, 3
15V	15V	>V_{ITRIP}	5V	0 (Note 2)	0	0
15V	15V	0V	0V	high imp	0	0

Notes: 1. A shoot-through prevention logic prevents LO1, 2, 3 and HO1, 2, 3 for each channel from turning on simultaneously.

2. UVCC is not latched, when V_{CC} > UVCC, FAULT returns to high impedance.

3. When ITRIP < V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ V_{CC}= 15 V).

■ TIMING DIAGRAM AND WAVEFORMS

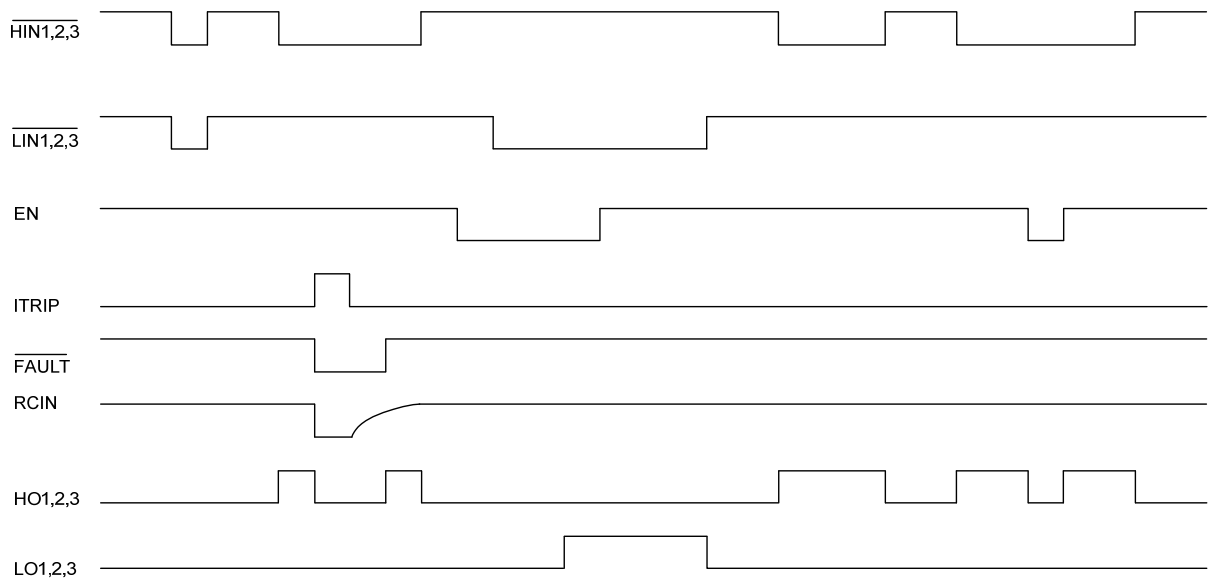


Figure 1. Input/Output Timing Diagram

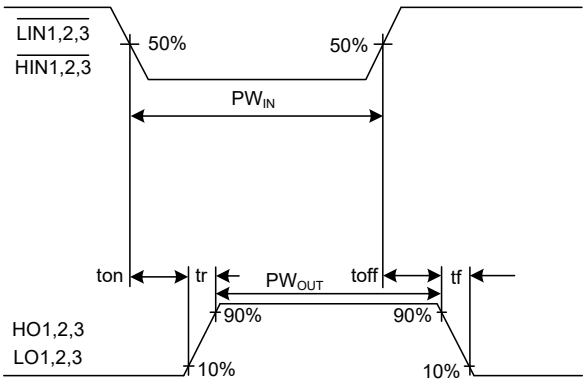


Figure 2. Switching Time Waveforms

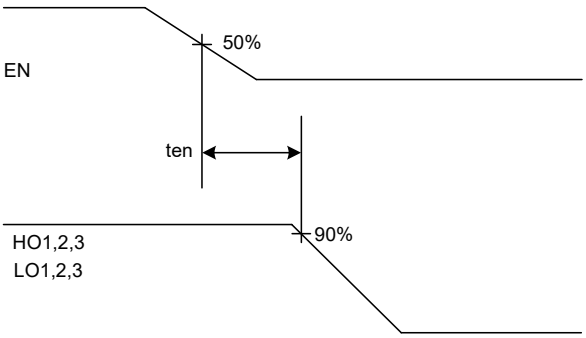


Figure 3. Output Enable Timing Waveform

■ TIMING DIAGRAM AND WAVEFORMS (Cont.)

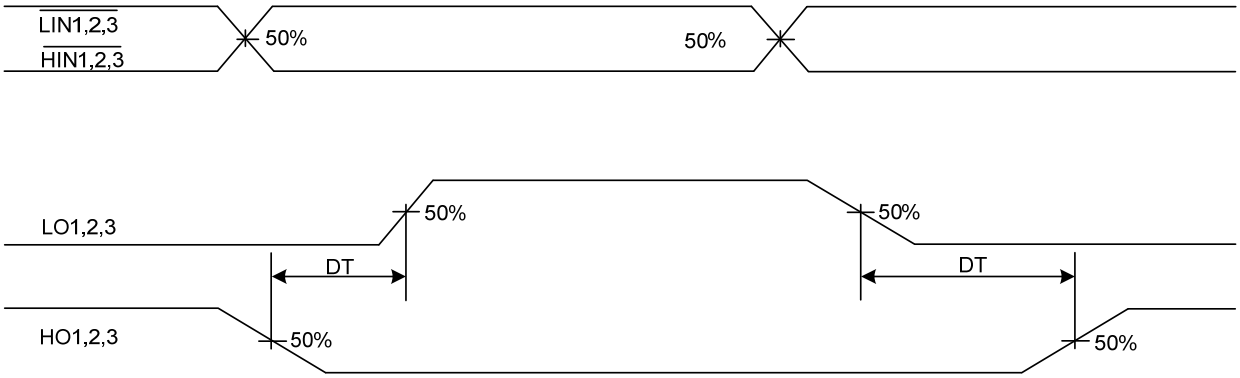


Figure 4. Internal Deadtime Timing Waveforms

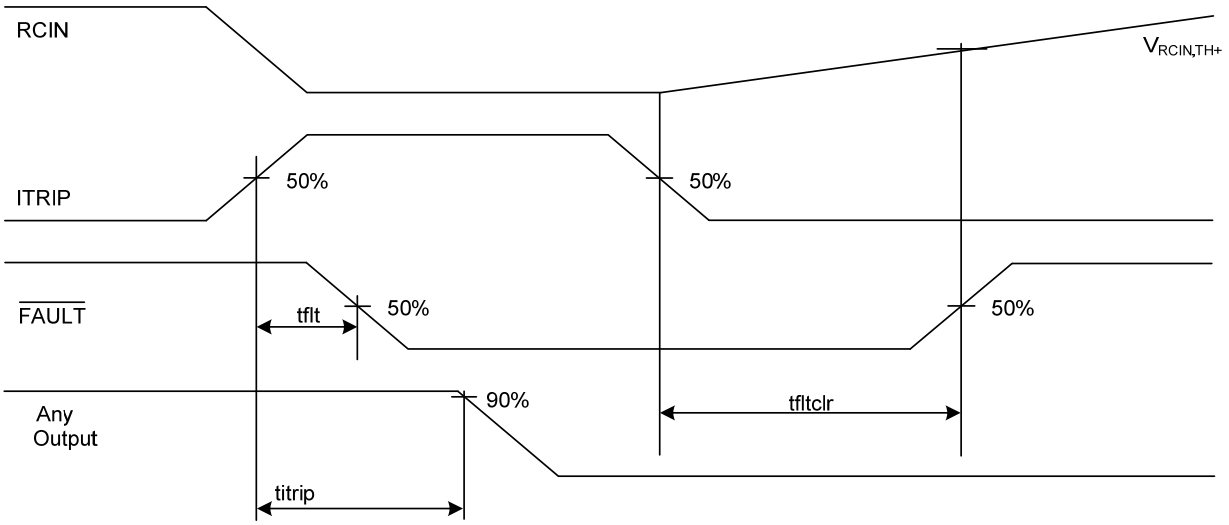


Figure 5. ITRIP/RCIN Timing Waveforms

■ TIMING DIAGRAM AND WAVEFORMS (Cont.)

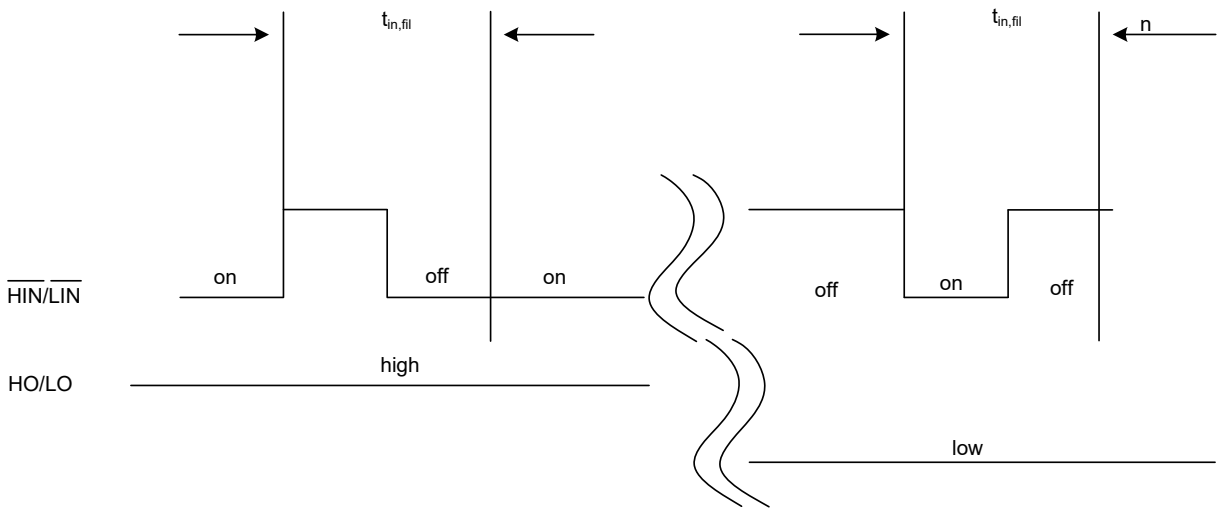


Figure 6. Input Filter Function

■ TYPICAL APPLICATION CIRCUIT