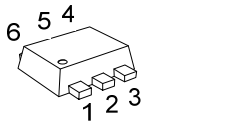
18V, 3A ,1.1MHZ SYNCHRONOUS STEP DOWN CONVERTER



SOT-563

■ DESCRIPTION

The UTC **UD18307** is an easy-to-use, 1.1MHz, synchronous step- down Buck converter, which integrated low on-resistance high-side and low-side power MOSFETs. The UTC **UD18307** can deliver 3A continues output current efficiently with excellent load and line regulation. The UTC **UD18307** adopts constant-on-time (COT) control operation, which provides very fast transient response, easy loop design, and very tight output regulation. The UTC **UD18307** has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open/short protection and thermal shutdown in case of excessive power dissipation. The UTC **UD18307** is available in an ultra- small SOT563 package and requires a minimal number of readily available, standard, external components.

■ FEATURES

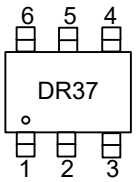
* 4.3V to 18V Input Voltage Range Supporting
* 20V Absolute Maximum Rating
* 3A Continuous Output Current
* Output Adjustable from 0.8V
*105mΩ and 60mΩ Internal Power MOSFETs
* 110μA Low Quiescent Current
* 1.1MHz Switching Frequency
* High-Efficiency Synchronous Mode Operation
* Internal Soft Start (SS)
* Over-Current Protection (OCP) and Hiccup
* Power-Save Mode (PSM) at Light Load
* Thermal Shutdown Protection

■ ORDERING INFORMATION

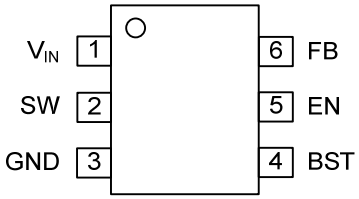
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD18307L-AN6-R	UD18307G-AN6-R	SOT-563	Tape Reel

UD18307G-AN6-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AN6: SOT-563 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



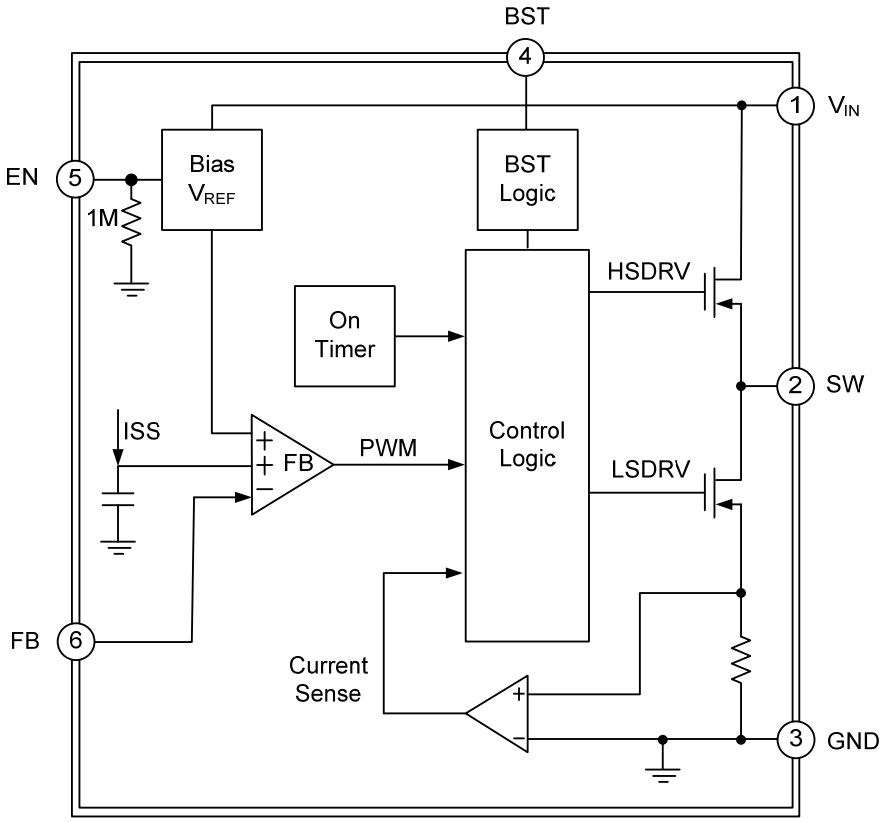
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	PIN	DESCRIPTION
1	V_{IN}	P	**Supply voltage.** The UTC **UD18307** operates from a 4.3V to 18V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at the input.
2	SW	O	**Output switching node.** Connect to power inductor.
3	GND	P	**System ground.** GND is the reference ground of the regulated output voltage. GND requires extra care during the PCB layout. Connect GND with copper traces and vias.
4	BST	O	**Bootstrap.** Connect a 0.1μF BST capacitor and a resistor between SW and BST to form a floating supply across the high- side switch driver.
5	EN	I	**On/off control.** High = on, Low = off. Precision enable input allows adjustable UVLO by external resistor divider.
6	FB	I	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. Never short this terminal to ground during operation.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	-0.3 ~ 20	V
SW to GND	V_{SW}	-0.3 ~ V_{IN}+0.3	V
EN to GND	V_{EN}	-0.3 ~ 20	μA
BST to SW	V_{BST-SW}	-0.3 ~ 6	V
All Other Pins		-0.3 ~ 6	V
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	4.3 ~ 18	V
V_{OUT} to GND	V_{OUT}	0.8 ~ V_{IN} × D_{MAX} (Note)	V
EN to GND	V_{EN}	0 ~ 18	V
Max. Continues Output Current	I_{LOAD}	3	A
Junction Temperature	T_J	-40 ~ +125	°C

Note: Guaranteed by design and engineering sample characterization.

■ THERMAL DATA (Note)

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	130	°C/W
Junction to Case	θ_{JC}	60	°C/W

Note: Measured on JESD51-7, 4-Layer PCB, and the PCB has no copper for thermal dissipation. Normal PCB with copper thermal resistance will be smaller.

■ ELECTRICAL CHARACTERISTICS (V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UVLO AND QUIESCENT CURRENT						
V_{IN} UVLO Rising Threshold	$V_{IN\_UV\_R}$			4.1	4.25	V
V_{IN} UVLO Hysteresis	$V_{IN\_UV\_Hys}$			300		mV
Quiescent Current	I_Q	V_{FB} =0.81V		110		μA
Shutdown Current	I_{SD}	V_{EN} = 0V		0.7		μA
FEEDBACK VOLTAGE						
Feedback Voltage	V_{FB}		784	796	808	mV
Feedback Current	I_{FB}			10	100	nA
FB UV Threshold	V_{UV_TH}	Hiccup entry		25%		V_{REF}
Hiccup Duty Cycle (Note)	D_{Hiccup}			15		%
POWER STAGE						
High-Side Switch on Resistance	R_{ON_HS}			105		mΩ
Low-Side Switch on Resistance	R_{ON_LS}			60		mΩ
High-Side Switch Leakage Current	I_{LKG_HS}				1	μA
Low-Side Switch Leakage Current	I_{LKG_LS}				1	μA
CURRENT LIMIT						
Valley Current Limit	I_{LIM}			3.8		A
SOFT START						
Soft-Start time	T_{SS}	V_{OUT} from 10% to 90%		0.75		ms
SWITCHING FREQUENCY/SYNC FUNCTION						
Oscillator frequency	F_{SW}			1100		kHz
Minimum On Time (Note)	T_{ON_MIN}			60		ns
Minimum OFF Time (Note)	T_{OFF_MIN}			220		ns
ENABLE						
Enable Rising Threshold	V_{EN_R}		2.20	2.32	2.44	V
Enable Threshold Hysteresis	V_{EN_Hys}			250		mV
Enable Input Current	I_{EN}	V_{EN}=2V		2		μA
Enable Input Resistor	R_{EN}			1		MΩ
THERMAL PROTECTION						
Thermal Shutdown (Note)	T_{OTP_R}			150		°C
Thermal Hysteresis (Note)	T_{OTP_Hys}			20		°C

Note: Guaranteed by design and engineering sample characterization.

■ FUNCTION DESCRIPTIONS

COT control loop operation

The **UD18307** is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range. After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS- FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS- FET off and HS-FET on period.

Light Load operation (PFM)

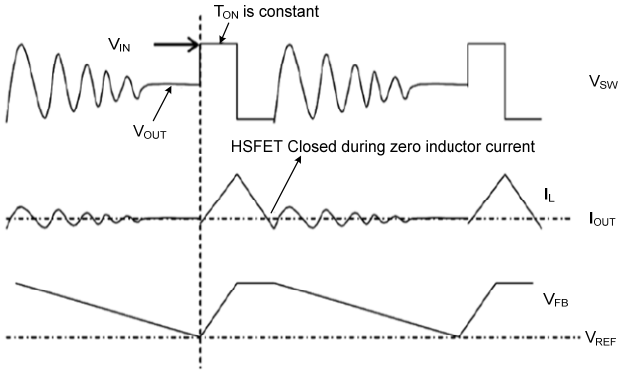


Figure 1. Light Load Operation

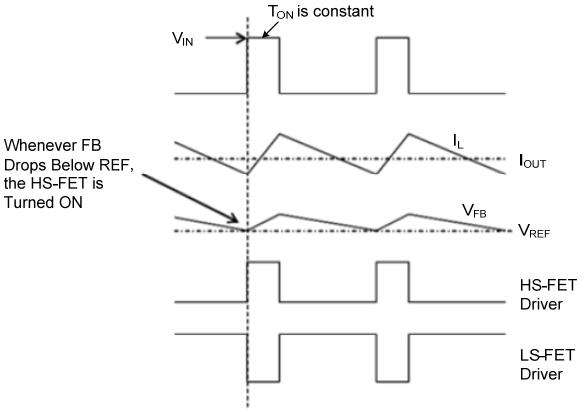


Figure 2. Heavy Load Operation

In light load condition, V_{FB} can't reach V_{REF} while the inductor current is approaching zero, a current modulator takes over control of the LS-FET and limits the inductor current around zero, and the LS-FET driver enters hi-z state since that time, the output drop speed is very slow, thus the **UD18307** reduces the switching frequency naturally, and high efficiency is achieved. As a trade-off, PFM mode suffers larger V_{OUT} ripple.

Heavy Load operation (CCM)

with the load current increasing, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly.

The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device enters CCM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

■ FUNCTION DESCRIPTIONS (Cont.)

Enable (EN) Control

The **UD18307** has a dedicated enable control pin with positive logic. Drive EN pin voltage higher than 2.32V(typical) to turn on the regulator, and drive EN pin voltage lower than 2.07V(typical) to turn it off. By using the two external resistor dividers, it is easy to optimize the start and stop voltage of the system via EN pin.

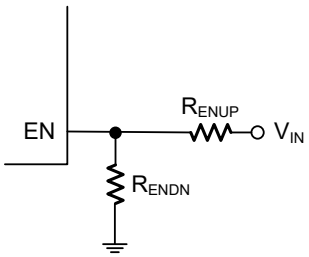


Figure 3. Heavy Load Operation

Start voltage Setting:

$$V_{START}=2.32\times\frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} \quad (2)$$

Stop voltage Setting:

$$V_{STOP}=2.07\times\frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} \quad (3)$$

Tie EN pin to VIN directly to set IC automatically start-up.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The **UD18307** UVLO comparator monitors the input voltage. The UVLO rising threshold is about 4.1V, while its falling threshold is consistently 3.8V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1.1V. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 0.75ms(10%~90%) internally.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The **UD18307** has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the high side will not turn on again. The output voltage drops until V_{FB} is below the under voltage (UV) threshold. Once UV is triggered, the **UD18307** enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

Pre-Bias Start-Up

The **UD18307** is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Output Over-Voltage Protection

The **UD18307** has implement output over-voltage protection. If output voltage rises above the regulated voltage, IC will stop switching to avoid the output voltage overshoot.

■ FUNCTION DESCRIPTIONS (Cont.)

Large Duty Cycle Operation

When **UD18307** will automatically extend the frequency to support the application when V_{IN} is close to V_{OUT}. The frequency extend circuit will be triggered when T_{OFF_MIN} time is reached. The **UD18307** can support up to 99% maximum duty cycle.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

■ APPLICATION INFORMATION

The **UD18307** output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.796V. The feedback network is shown below Figure.

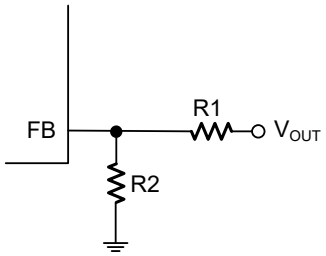


Figure 4. Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2} \quad (4)$$

Selecting the Inductor

For most applications, use a 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a small DC resistance.

For most designs, the inductance value can be derived from Equation:

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times f_{SW}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L\_MAX}=I_{LOAD}+\frac{\Delta I_L}{2} \quad (6)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1. Resistor Selection for Common Output Voltages (Note)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)
5	11.5	2.2	4.7	22
3.3	6.98	2.2	4.7	22
2.5	4.75	2.2	3.3	22
1.8	2.8	2.2	2.2	22
1.5	1.96	2.2	2.2	22
1.2	1.13	2.2	1.5	22
1.05	0.715	2.2	1.5	22

Note: For a detailed design circuit, please refer to the Typical Application Circuits.

■ APPLICATION INFORMATION (Cont.)

Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

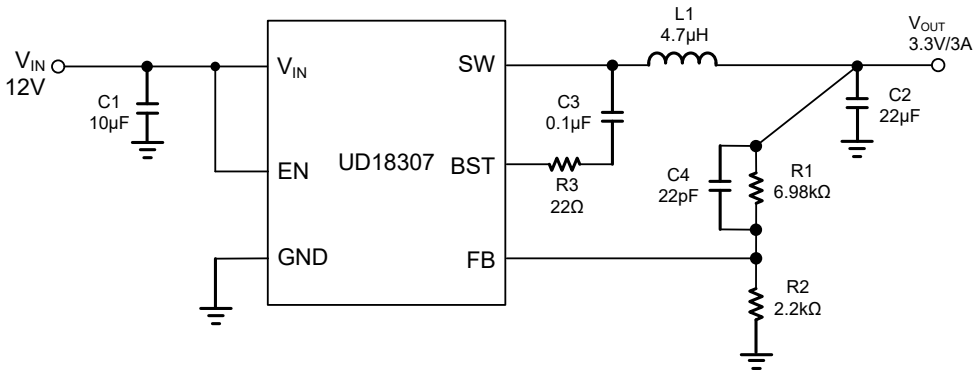
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

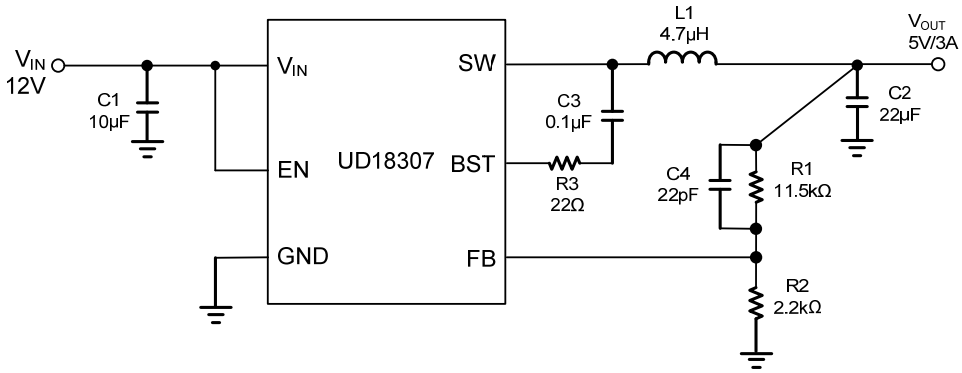
The characteristics of the output capacitor also affect the stability of the regulation system. The **UD18307** can be optimized for a wide range of capacitance and ESR values.

■ TYPICAL APPLICATION CIRCUIT

V_{IN}=12V, V_{OUT}=3.3V/3A



V_{IN}=12V, V_{OUT}=5V/3A



Note: C4 is optional for better transient performance.