



UT30N15M

Power MOSFET

30A, 150V N-CHANNEL POWER MOSFET

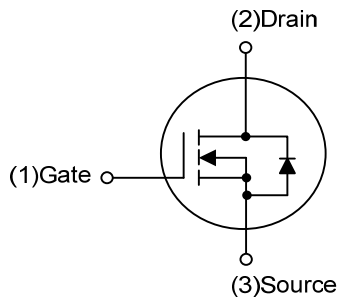
DESCRIPTION

The UTC **UT30N15M** is a N-Channel enhancement mode power field effect transistors using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

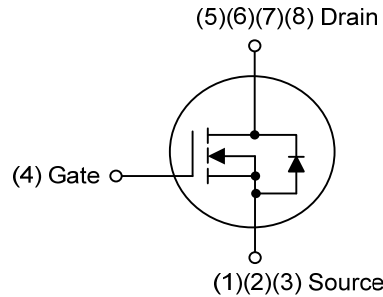
FEATURES

- * $R_{DS(ON)} \leq 54 \text{ m}\Omega @ V_{GS}=10V, I_D=15A$
- * $R_{DS(ON)} \leq 57 \text{ m}\Omega @ V_{GS}=4.5V, I_D=15A$
- * Improved dv/dt capability
- * High Switching Speed
- * Fast switching

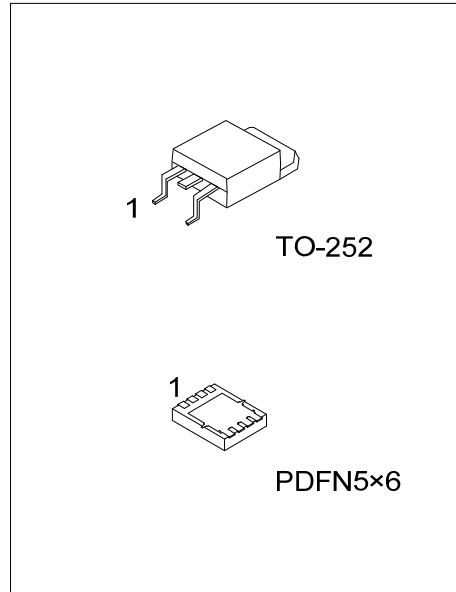
SYMBOL



TO-252



PDFN5x6



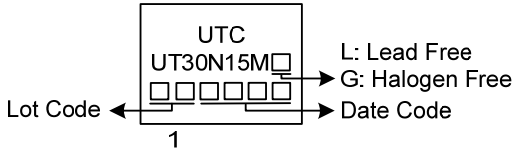
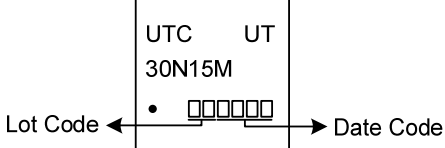
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT30N15ML-TN3-R	UT30N15MG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT30N15ML-P5060-R	UT30N15MG-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT30N15MG-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252, P5060: PDFN5x6</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

TO-252	PDFN5x6
 <p>Diagram of TO-252 marking: A rectangular box contains the text 'UTC' and 'UT30N15M' followed by a small square. Below this is a row of five small squares. An arrow labeled 'Lot Code' points to the first square from the left. An arrow labeled 'Date Code' points to the last square from the right. Below the row of squares is the number '1'. To the right of the box, the text 'L: Lead Free' and 'G: Halogen Free' is present, with arrows pointing to the right.</p>	 <p>Diagram of PDFN5x6 marking: A rectangular box contains the text 'UTC UT' and '30N15M' followed by a small square. Below this is a row of five small squares with a dot to the left of the first square. An arrow labeled 'Lot Code' points to the first square from the left. An arrow labeled 'Date Code' points to the last square from the right.</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	150	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous ($V_{GS}=10\text{V}$)	I_D	30	A
	Pulsed (Note 2)	I_{DM}	60	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	22	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.08	V/ns
Power Dissipation	TO-252	P_D	46	W
	PDFN5x6		14	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 21\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
	PDFN5x6		83	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-252	θ_{JC}	2.7	$^{\circ}\text{C}/\text{W}$
	PDFN5x6		8.9	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

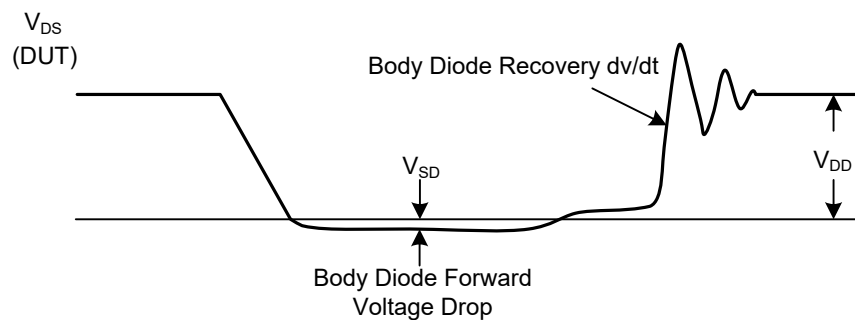
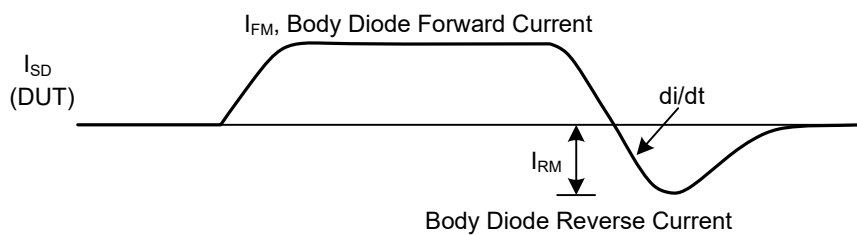
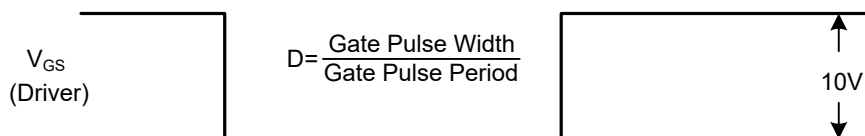
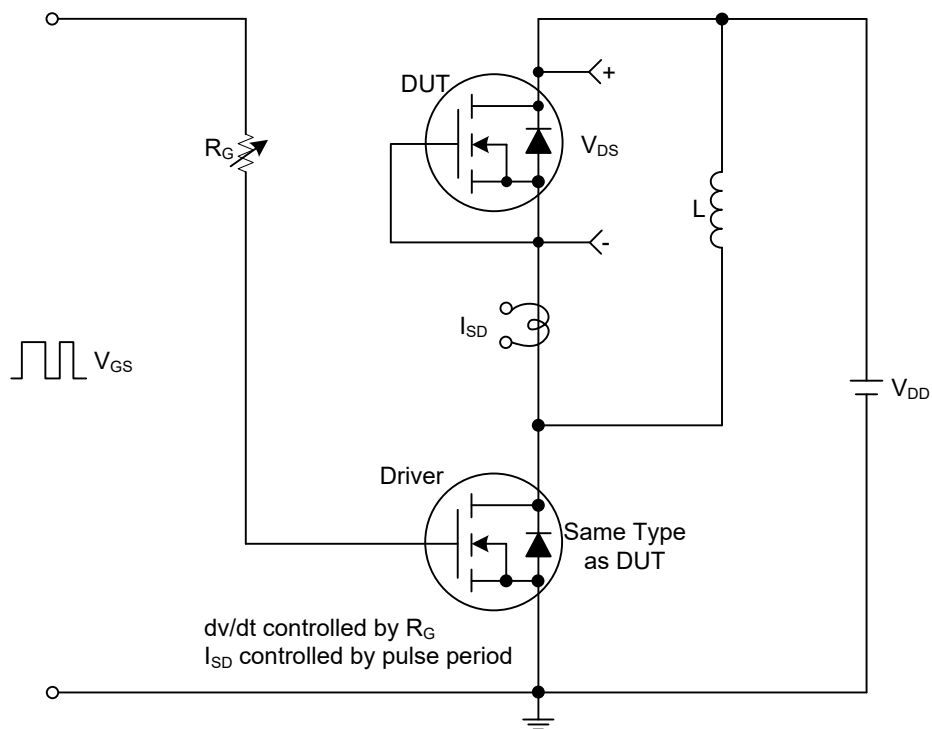
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	150			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =150V, V _{GS} =0V			10	μA
Gate- Source Leakage Current	Forward	I _{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =15A			54	mΩ
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =15A			57	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		4404		pF
Output Capacitance	C _{OSS}			192		pF
Reverse Transfer Capacitance	C _{RSS}			130		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =100V, V _{GS} =10V, I _D =30A (Note 2)		108		nC
Gate to Source Charge	Q _{GS}			31		nC
Gate to Drain Charge	Q _{GD}			16		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =75V, V _{GS} =10V, I _D =30A, R _G =25Ω, (Note 2)		42		ns
Rise Time	t _R			40		ns
Turn-OFF Delay Time	t _{D(OFF)}			283		ns
Fall-Time	t _F			130		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				30	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				60	A
Drain-Source Diode Forward Voltage	V _{SD}	I _S =30A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time	t _{rr}	I _F =30A, V _{GS} =0V, di/dt=100A/μs		80		ns
Body Diode Reverse Recovery Charge	Q _{rr}			256		nC

Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

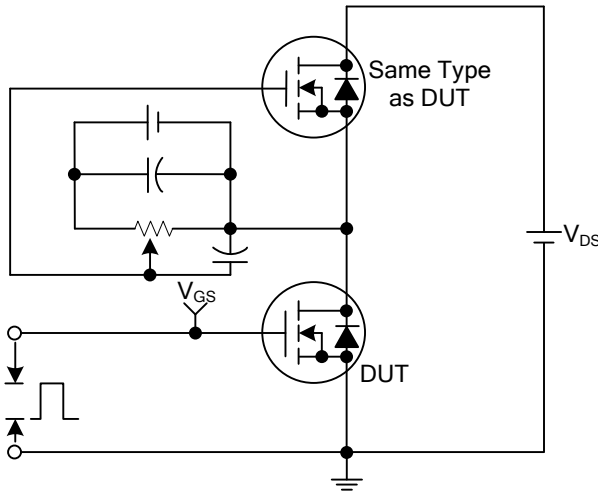
2. Essentially independent of operating ambient temperature.

TEST CIRCUITS AND WAVEFORMS

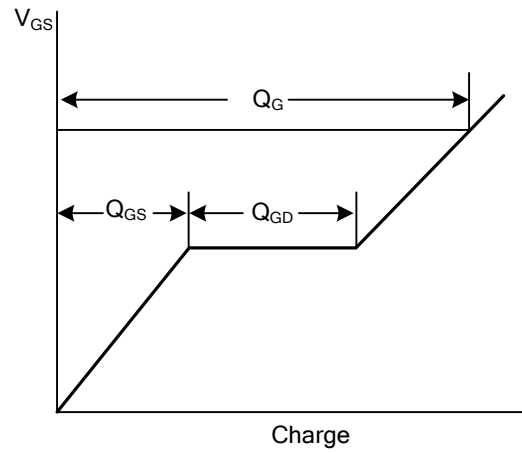


Peak Diode Recovery dv/dt Test Circuit and Waveforms

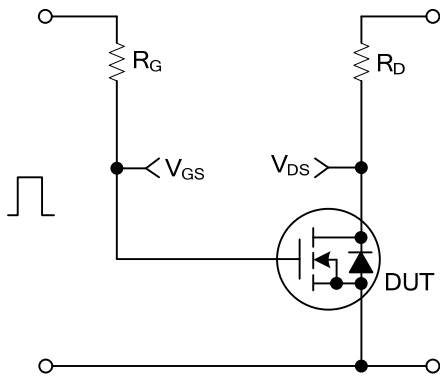
TEST CIRCUITS AND WAVEFORMS



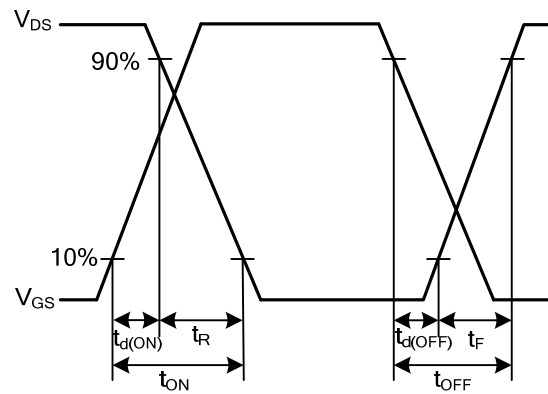
Gate Charge Test Circuit



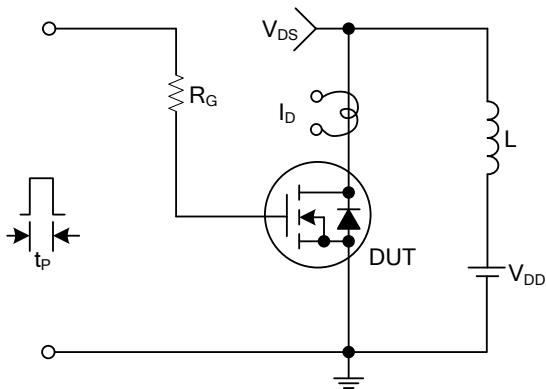
Gate Charge Waveforms



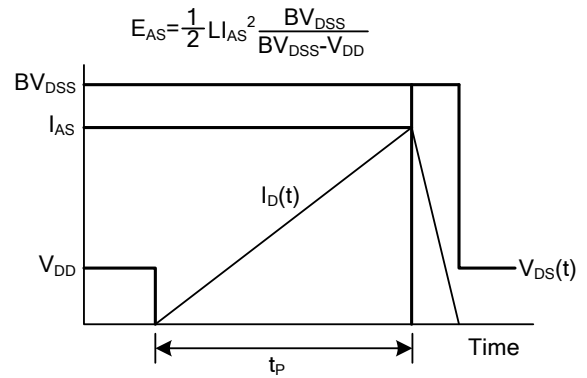
Resistive Switching Test Circuit



Resistive Switching Waveforms

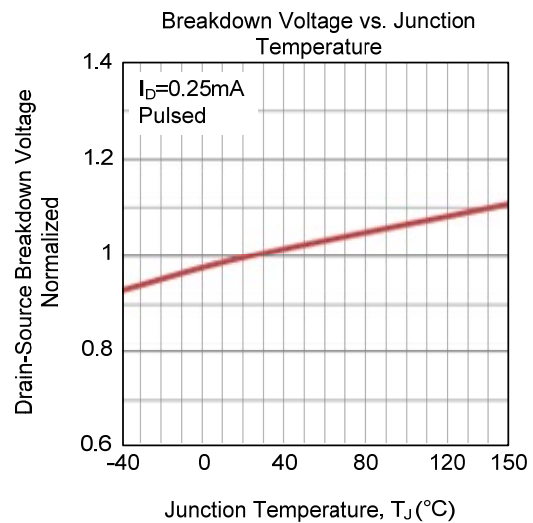
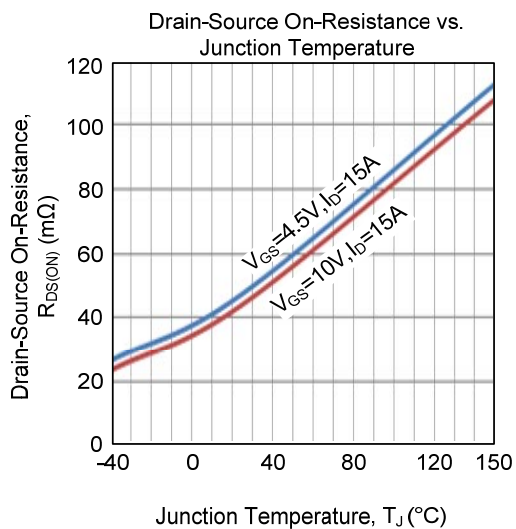
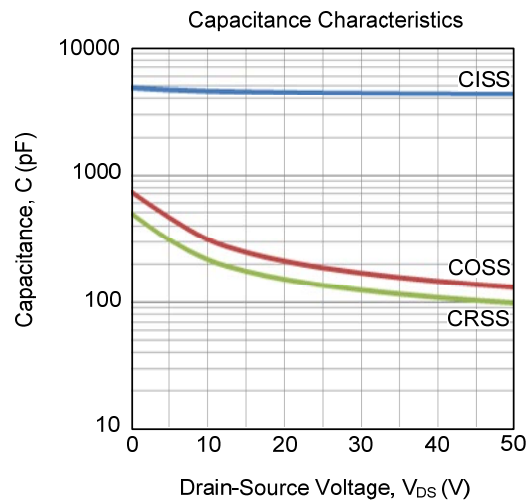
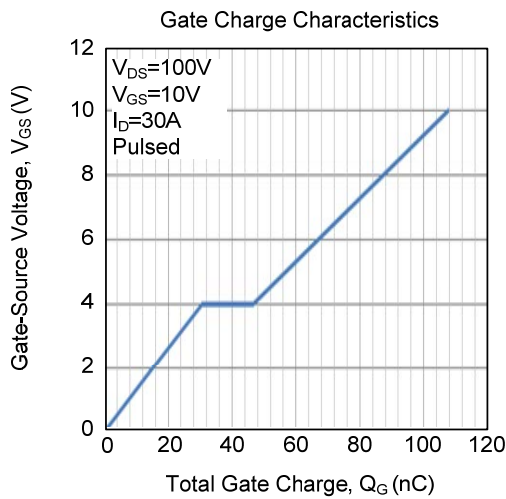
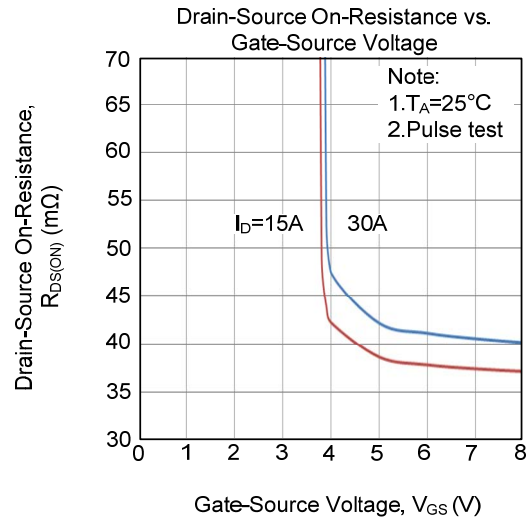
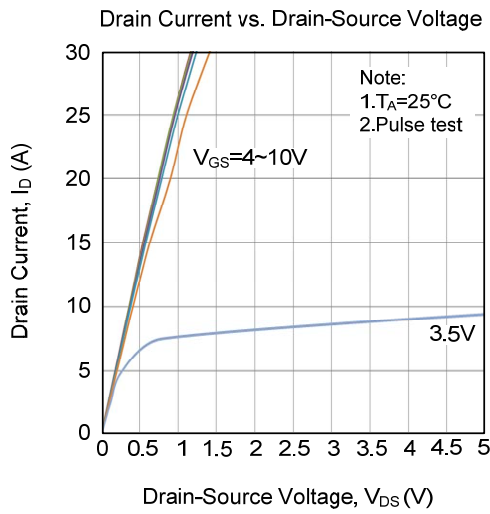


Unclamped Inductive Switching Test Circuit

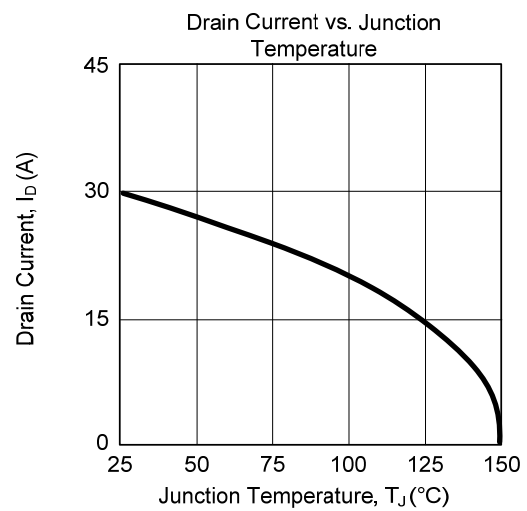
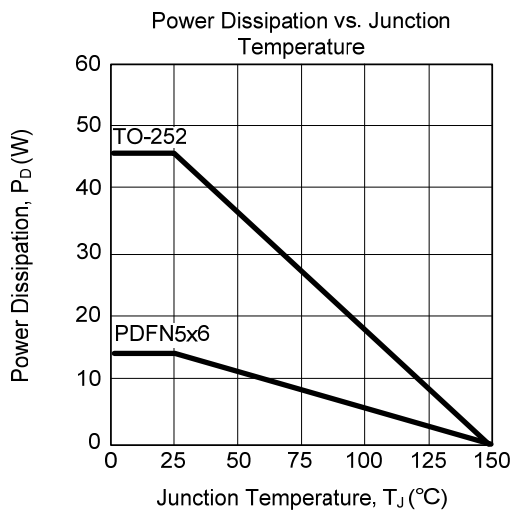
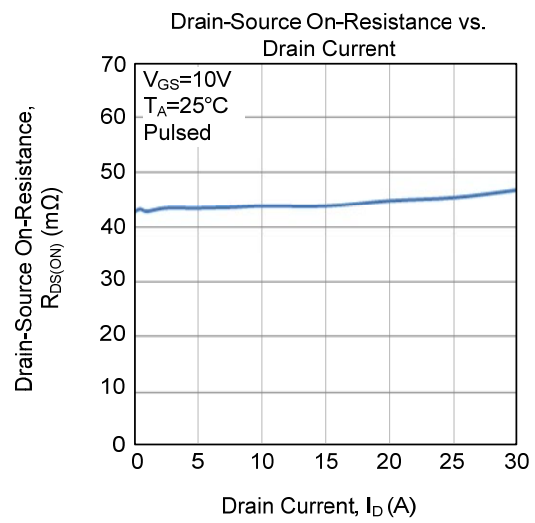
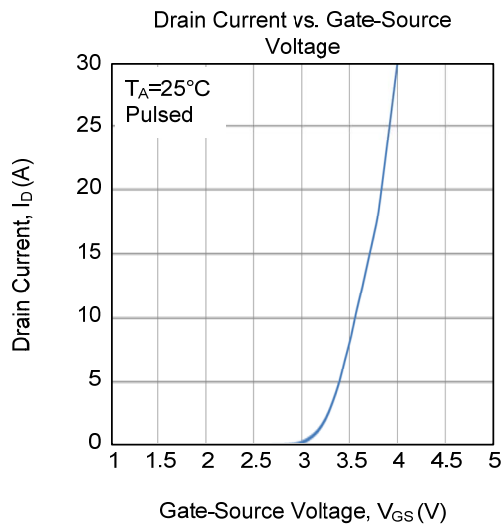
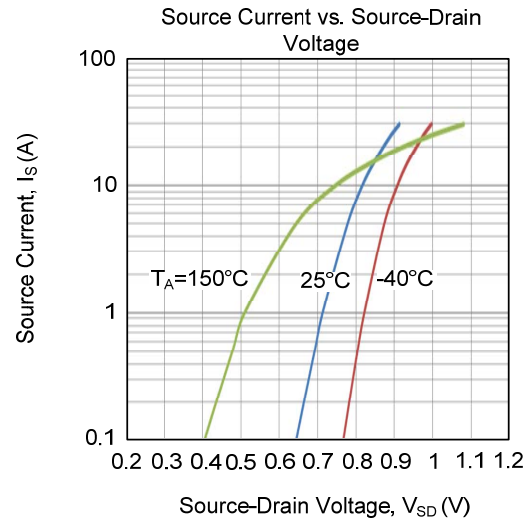
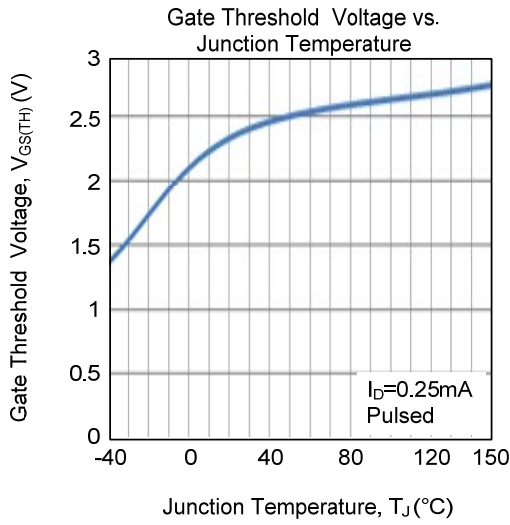


Unclamped Inductive Switching Waveforms

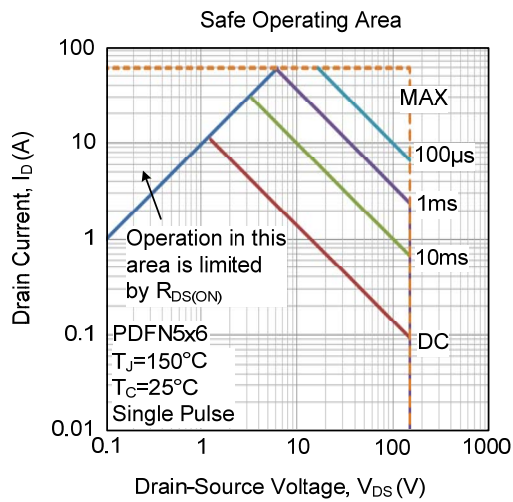
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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